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Hysteresis control of parallel-connected hybrid inverters

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THESIS

HYSTERESIS CONTROL OF PARALLEL-CONNECTED HYBRID INVERTERS

by

Bradford P. Bittle

September 2005

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13. ABSTRACT (maximum 200 words)

Integrated Power Systems will be used on future naval combatants. These systems will allow unprecedented control of shipboard power to propel the ship, sense the battle-space, and engage the enemy. One crucial enabling technology is robust power conversion modules like the hybrid dc to ac inverter. This thesis is a further exploration of the hybrid inverter scheme consisting of a six-step voltage-source inverter (VSI) and a hysteresis controlled current-source inverter (CSI). The six-step controller was redesigned to make it independent of the hysteresis controller. The hysteresis controller is fed a reference signal extracted from the total output current. The signal is filtered and modified by the closed-loop system such that the total output current approaches a perfect sine wave limited only by bandwidth. The modified closed-loop controller was compared to a previous Naval Postgraduate School effort and found to improve current total harmonic distortion from 3.2% to 1.8%. This thesis proves that existing power electronic technology can be used to produce high-fidelity waveforms for high-power Naval Propulsion Drives (50-100 MW).

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HYSTERESIS CONTROL OF PARALLEL-CONNECTED HYBRID INVERTERS

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Submitted in partial fulfillment of the
requirements for the degree of

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ABSTRACT

Integrated Power Systems will be used on future naval combatants. These systems will allow unprecedented control of shipboard power to propel the ship, sense the battle-space, and engage the enemy. One crucial enabling technology is robust power conversion modules like the hybrid dc to ac inverter. This thesis is a further exploration of the hybrid inverter scheme consisting of a six-step voltage-source inverter (VSI) and a hysteresis controlled current-source inverter (CSI). The six-step controller was redesigned to make it independent of the hysteresis controller. The hysteresis controller is fed a reference signal extracted from the total output current. The signal is filtered and modified by the closed-loop system such that the total output current approaches a perfect sine wave limited only by bandwidth. The modified closed-loop controller was compared to a previous Naval Postgraduate School effort and found to improve current total harmonic distortion from 3.2% to 1.8%. This thesis proves that existing power electronic technology can be used to produce high-fidelity waveforms for high-power Naval Propulsion Drives (50-100 MW).

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LIST OF SYMBOLS, ACRONYMS, AND ABBREVIATIONS

AEPS	Advanced Electric Propulsion System
CRS	Congressional Research Service
CSI	Current-Source Inverter
FPGA	Field Programmable Gate Array
GIC	Generalized Impedance Converter
GTO	Gate-Turn-Off Transistors
IEEE	Institute of Electrical and Electronics Engineers
IGBT	Insulated Gate Bipolar Transistor
IPS	Integrated Power System
MCT	MOS-Controlled Thyristors
MOSFET	Metal-Oxide-Silicon Field Effect Transistor
MTBF	Mean Time Between Failure
NAVSEA	Naval Sea Systems Command
NDIA	National Defense Industrial Association
NRAC	Naval Research Advisory Committee
ONR	Office of Naval Research
PCHI	Parallel Connected Hybrid Inverters
PEBB	Power Electronics Building Blocks
PLD	Programmable Logic Device
SSGTG	Ship’s Service Gas Turbine Generators
THD	Total Harmonic Distortion
VSI	Voltage-Source Inverter

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I would like to extend this opportunity to recognize the people who provided me the guidance and opened the doors of knowledge to allow this research to be completed.

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And finally, thanks to my wife, Marietta, and my children, Ian, Maeve, and Caroline, for all of your love and support. Without you none of my efforts would mean as much.

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EXECUTIVE SUMMARY

This thesis continues previous work conducted at the Naval Postgraduate School. The inverters previously used were replaced with commercially available 20 kVA Semikron IGBT PEBBs, which have three half-bridges rated at 50A/1200V and an IGBT/diode brake for protection. The unit is able to produce its own dc bus using an installed, uncontrollable three-phase diode rectifier module. The Semikron SKHI 22B drivers were used to gate the half-bridges. The bulk controller was replaced with a shift register driven six-state machine. The bulk inverter currents for all three phases were measured using Hall-effect sensors and passed through a low-pass filter and a phase correcting all-pass filter to create the hysteresis reference waveforms. These waveforms were passed to the modified and expanded hysteresis controller. Finally the hybrid inverter was constructed and tested to determine the operational efficacy of the new layout and redesigned controllers.

An overview of the major concepts explored is provided in and the designs used to implement the bulk six-step and the hysteresis controllers are presented. Specific designs covered include: the bulk six-step controller, the Hall Effect sensor circuit, the filter circuit, and the modified hysteresis circuit. The controller design for this thesis produces a 60 Hz output of the bulk controller and generates a manually adjustable phase and gain correction to tune the reference waveform for the hysteresis controller. The ideal bulk controller would allow variable system frequencies. The ideal hysteresis controller would sense the system frequency and automatically adjust the gain and phase correction of the reference waveform to match the load current. The use of a Field Programmable Gate Array (FPGA) or a Programmable Logic Device (PLD) would simplify the construction of this controller type and allow variable frequency operation of the bulk inverter.

A SIMULINK model was used to evaluate the new control strategy. The outputs of the bulk controller matched the predicted values. The output of the hysteresis inverter produces a current waveform which precisely cancels the harmonic content of the bulk inverter. A quick harmonic check obtained by summing the currents of all three output

phases shows that there is very little harmonic content in the output. The computer model demonstrates the circuit designed will improve the performance of the Parallel-Connected Hybrid Inverter (PCHI) to meet IEEE STD 519 requirements.

The results of the laboratory prototype PCHI system generally support the theoretical results provided by the simulation. Differences observed between theory and actual laboratory results were caused by the unbalanced load, the width of the hysteresis band, filter mismatches, and the 60Hz (low-frequency) transformer. The load was left slightly unbalanced to replicate the "real-world" application of the controller. Other areas of the controller could be changed to improve the fidelity of the load current, as listed below.

First, the hysteresis band can be reduced to a smaller value by replacing components in the hysteresis circuit. To create the hysteresis tolerance band, 0.051V is added and subtracted to the 6V reference wave to create the tolerance band. The resultant band was approximately 1.7%. If the tolerance band were reduced to 1%, the load current fidelity would be improved. The switching frequency of the hysteresis controller would increase from the 5 kHz observed. The 20 kHz PEBB switching limit will allow a smaller tolerance band. Further research could investigate tolerance band versus maximum switching frequency.

Second, the three filters can be tuned to optimize the output. Once the filters were installed in the circuit they were not adjusted further to match either the unbalanced load or to correct for the actual bulk inverter operating frequency. Manually tuning the filters would be a time consuming process with the filter topology used in this thesis. Future research should focus on replacing the filter with one that detects the bulk inverter output frequency, optimizes the cut-off frequency, and automatically phase and gain corrects the LPF output. This will ensure that a nearly idealized reference waveform is constantly phase and gain locked to the load current.

Third, the antagonistic action between the hysteresis inverter and the bulk inverter through the coupling transformers adds unwanted broadband noise. An optimization of the reactances in the circuit will need to be analyzed to correct this phenomenon. The

bulk inverter and hysteresis inverter interface may require an additional filter to improve the fidelity of the hybrid inverter output. Even without correction the overall load current THD improvement is exceptional

Fourth, the use of the dq0-reference frame would simplify the control topology and enable the use of an FPGA more easily. The conversion to the stationary dq0-reference frame would provide a more responsive and robust controller. The FPGA construct opens the possibility of programming a chip to perform the complex mathematics to transform from one reference frame to another while automatically adjusting the filter parameters.

The PCHI prototype performance validates the use of a hysteresis controlled inverter to filter the load current generated by a bulk inverter. The resultant load current demonstrates the reduction in harmonic content from the raw bulk inverter current. This reinforces the findings of Reference 10.

The spread spectrum nature of the modulation and the uncertainty (random nature) of a switching event, make this system ideal for stealth operation. When coupled with a variable frequency bulk inverter, shipboard loads can be driven at the most efficient frequency of operation and reduce the predominately 50Hz, 60Hz and 400Hz tonals onboard allied warships. An ideal first application would be to replace the dc-to-ac motor-generator sets in the fleet. These are maintenance intensive and are a significant life-cycle cost-driver. A solid-state power converter would reduce the maintenance requirements of the system and would significantly reduce the life-cycle costs of the platform in the long run. The significant initial investment would pay for itself many times over in reduced maintenance over a thirty year life span.

The six-step controller was simplified and the new design performed well at approximately 60 Hz. Both the modified hysteresis controller and the bulk controller were able to operate the Semikron PEBBs. The hysteresis controller filter produced three nearly ideal sinusoids from the sensed phase load currents to generate reference waveforms for use by the hysteresis circuit. The single phase hysteresis controller test demonstrated that the switching frequency relationship with the reference signal was

valid. The SIMULINK model demonstrated that the new control strategy was valid and would potentially reduce the harmonic content of the load current. Finally the laboratory constructed PCHI provided solid proof that the hysteresis controlled inverter is a very capable active filter for the bulk inverter. The observed PCHI-generated load current THD was 1.81% which exceeds the IEEE Std. 519 (1999) limit of 2.5%. The PCHI system constructed in this thesis provides a simple method to filter the harmonic content from an inductive load. This thesis proves that existing technology can be used to produce high-fidelity waveforms for high-power Naval Propulsion Drives (50-100 MW). This conclusion is based on the bulk inverter providing 100% of the real power while the hysteresis inverter acts as an active filter.

I. INTRODUCTION

A. OVERVIEW

In January 2000, the Secretary of the Navy selected electric drive to propel all future classes of Navy warship. He stated that, "Changes in propulsion systems fundamentally change the character and the power of our forces. This has been shown by the movement from sails to steam or from propeller to jet engines… More importantly, electric drive, like other propulsion changes, will open immense opportunities for redesigning ship architecture, reducing manpower, improving ship life, reducing vulnerability and allocating a great deal more power to war-fighting applications." The next generation combatant, the DD(X), will be constructed with an Integrated Power System (IPS) to utilize all available shipboard power more efficiently and to unlock propulsion power for high-powered electric weapons and advanced sensors [1].

Over the last century the Navy has seen several transformational events that have changed the war-fighting character of the navy. The creation of the submarine provided unparalleled offensive power to the modern fleet. The advent of the flight deck and the development of the aircraft carrier provided the means to fight and win World War Two. The implementation of nuclear power transformed both the aircraft carrier and submarine into ideal offensive weapons with unlimited tactical flexibility. Indeed, nearly eighty five years after the USS Langley (CV-1) set sail and fifty years after the USS Nautilus (SSN-571) sent the message "Underway on Nuclear Power," the US Navy has been shaped by these transformational technologies.

Surprisingly, the method of shipboard power distribution has remained relatively unchanged over the last century even though electrical power demand has increased significantly (Fig. 1). Propulsive power is provided by one set of prime movers and the ship service and combat system loads are powered by a completely separate set of electric power generating equipment. There were instances, early in the last century, where warships were powered by turbo-electric drive to test the efficacy of propelling warships with electric motors instead of the then prohibitively expensive mechanical system requiring reduction gears. Table 1 provides a list of some of the more notable instances.

As industrial mechanical skills improved and reduction gears became more affordable, the US Navy shifted to the segregated propulsion plant turbine scheme used predominantly in the fleet today.

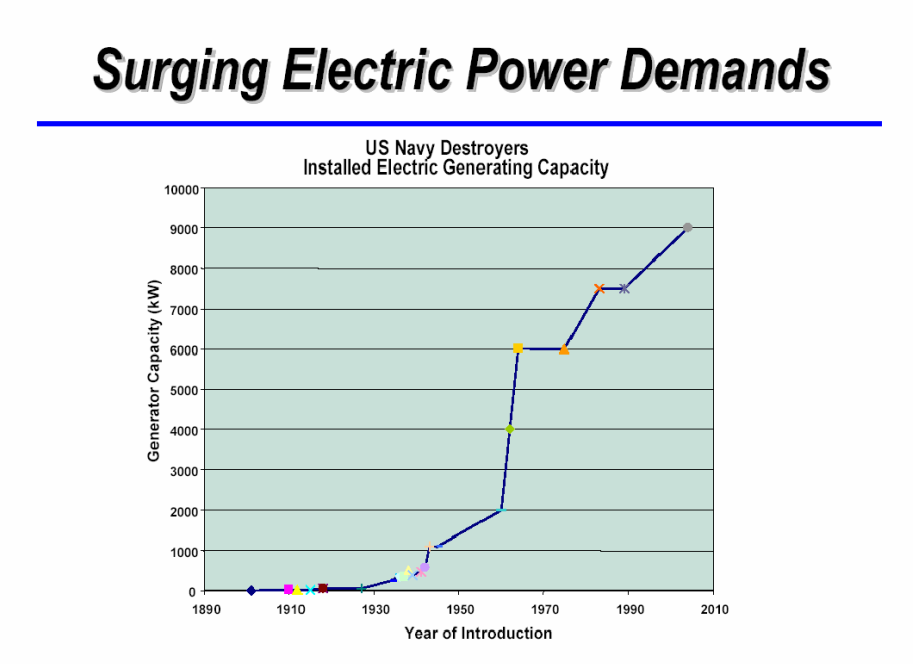

Figure 1. Historical Electric Power Generating Capabilities [From Ref. 2]

CV1, 2 x 3500 HP Induction Motor, Turbo-electric, 1913
Maryland Class BBs, 31,000 HP, Turbo-electric, 1920
CV2 and CV3, 8 x 22,500 HP Induction Motor, Turbo-electric, 1925
Fulton Class AS, 11,800 HP, Diesel-electric, 1940
DEs, Rudderow/Buckley/Butler/Canon Classes, 12,000 HP and 6,000 HP, Turbo- and Diesel-electric
Fleet Boats (SS)
USS Hunley, AS-31, 15,000 HP Synchronous, Diesel-electric, 1959
USS Tullibee, SSN-597, 2500 HP, Turbo-electric, 1960
USS Lipscomb, SSN-685, Turbo-electric, 1973
AGS/AGOR/T-ARC/T-AGS Classes, 800-5000 HP, AC-SCR-DC Motor, 1970s-Present

Table 1. USN Electric Drive Evolution [After Ref. 2]

During World War Two, the availability of adequate machine shops to manufacture enough geared turbines and reduction gears was inadequate to complete all of the ships then under construction. Certain classes of ship were constructed using turbo-electric drive simply so that they could be completed in time to fight the war. In most instances the electric drive ships outperformed their mechanical drive counterparts in

speed and endurance. Additionally, these turbo-electric ships were more compartmentalized and were therefore able to withstand more damage due to more robust ship architecture. However, the inherent complexity of electric machinery repair and the risk of power loss immediately following battle damage (due to short circuits caused by progressive flooding) drove designs back to the traditional mechanical drive propulsion plant. A more detailed history of electric drive in the US Navy can be found in References 3 and 4.

The Arleigh Burke class destroyers use four LM-2500 gas turbines to create nearly 79 MW of power to propel the ship through the water. Three separate Allison Ship Service Gas Turbine Generators, (SSGTG), produce 7.5 MW to power all ship service and combat loads (Fig. 2) [5]. For a large portion of the ship's lifetime the vast majority of the available propulsive power is unused because the ship does not cruise at the maximum available design speed but at a moderate eleven to fifteen knots. In addition, these legacy systems are increasingly vulnerable to combat damage, are expensive to maintain, and have no excess power capacity to supply next generation electromagnetic weapon systems. An identical ship built with an IPS would require two 35 MW main turbine generators and two auxiliary 4 MW gas turbine generator to produce 78 MW total power [5]. This would provide reconfigurable power which can be redirected on the fly to deliver power where the tactical situation requires. The Commanding Officer is given unprecedented flexibility to tailor his ship's electric configuration to meet his immediate need, whether it is to fight, to maneuver, or to combat battle damage after action (Fig. 3).

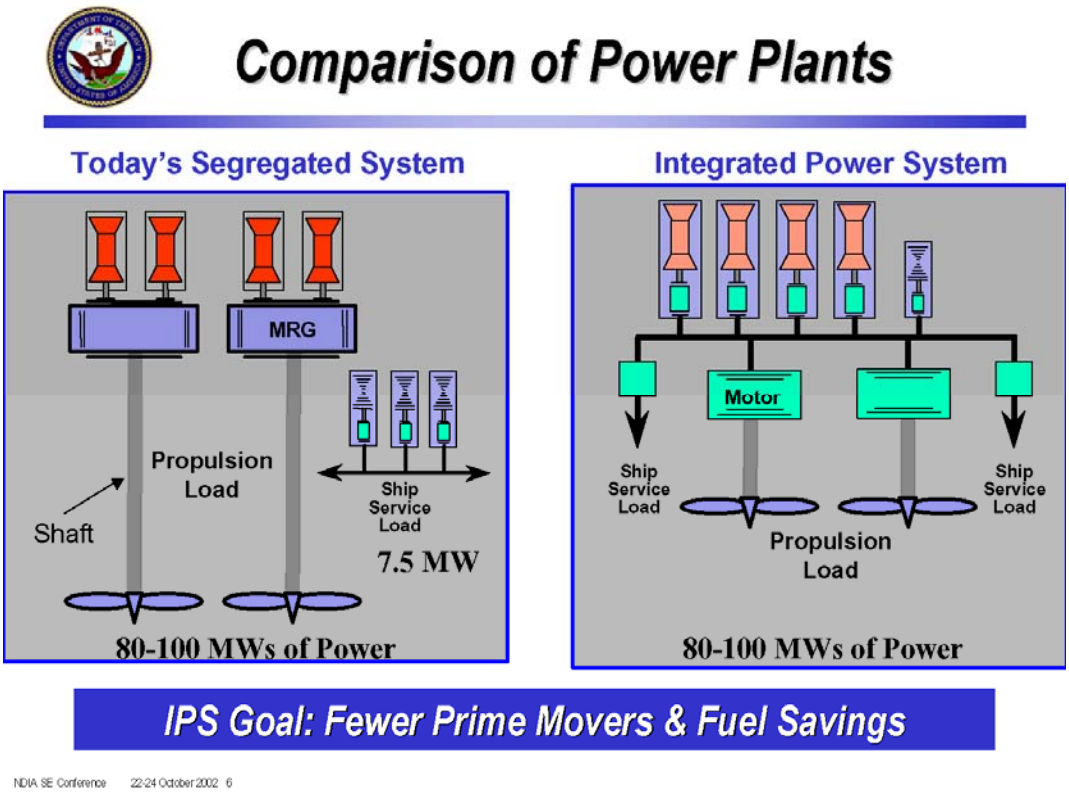

Figure 2. Conventional Propulsion versus IPS [From Ref. 5]

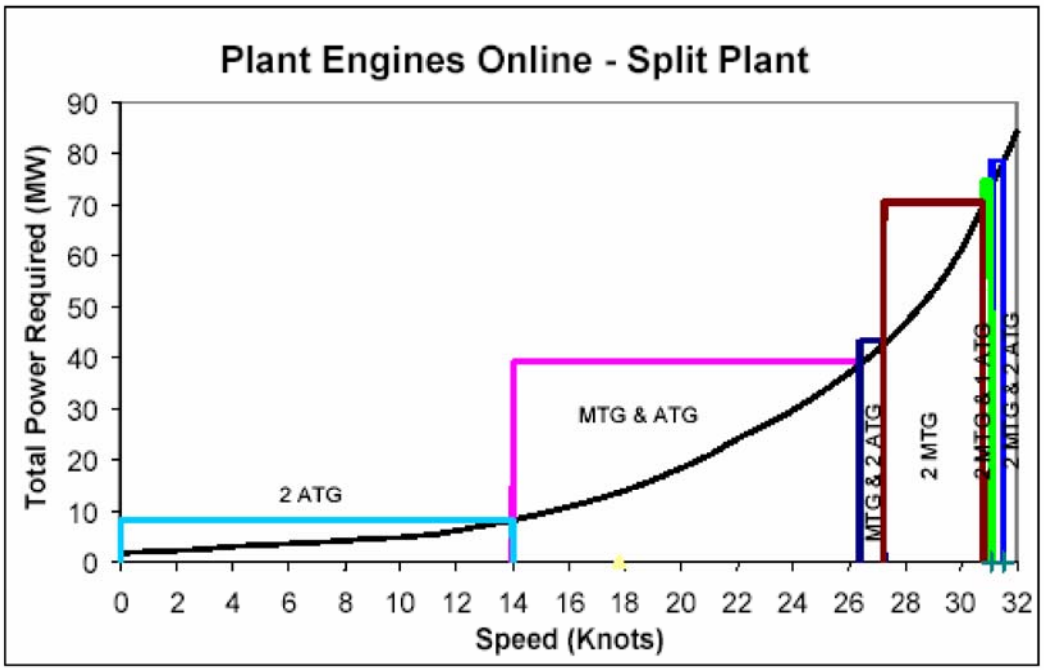

Figure 3. IPS Energy Management [From Ref. 2]

The benefits of using IPS are [6]:

- Signature Reduction: Less prime mover machinery equates to reduced infrared and acoustic signatures.
- Fuel Savings: Anticipated 15-20 % savings in fuel consumption over the life of the ship. A smaller propulsion plant is required to produce greater available power. Power generators online match ship's load requirements.
- Cheaper Construction: Reduced ship construction costs due to the modular nature of the IPS architecture. Additionally the modular design allows for quicker repair and modernization over the life of the ship. Reduced ship's displacement equates to higher maximum speed or greater payload capacity.
- Reduced Life-cycle Costs (up to 50%): Longer Mean Time Between Failures (MTBF) of propulsion components. Less manpower required to operate machinery.
- Increased Survivability: Shorter electric motor drive shaft compared to mechanical drive propulsion shafting allows for increased propulsion system compartmentalization, resulting in increased ship survivability.
- Simpler Systems: Eliminates costly hydraulic and pneumatic operated systems in favor of more cost-effective electro-mechanical systems and actuators. Allows one common method of power implementation.
- Enabler for Tomorrow's Weapons: Next generation pulsed and high power weapons systems due to increased load sharing between all shipboard systems.

The Office of Naval Research (ONR) is working with industry to produce one electronics package, the Power Electronics Building Block (PEBB), that will convert ac to dc, buck and/or boost dc to dc, convert ac from one frequency to another, and invert dc back to ac. PEBBs are pre-engineered, pre-tested, "plug and play" building blocks for high power controllers that are made multifunctional through software programmed controllers (Fig. 4) [4, 7].

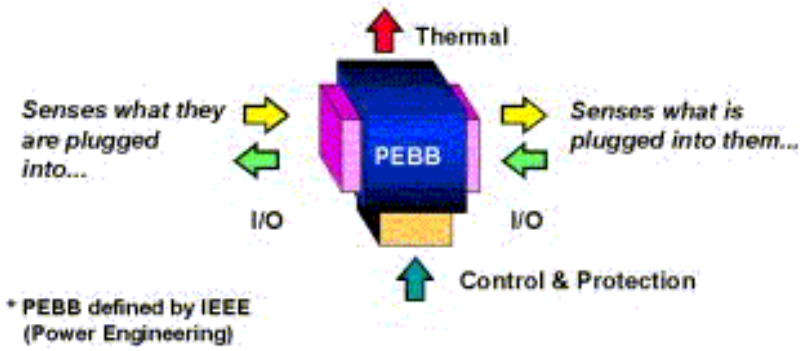

Figure 4. Power Electronics Building Blocks [From Ref. 4]

The use of PEBB technology utilizes the same principles of modularity and design which have allowed remarkable advances in the telecommunications and computer industries. The modules will be microprocessor controlled and will sense adjacent power system components to control and protect the module and the equipment on the bus. The PEBB concept will create a set standard in building block layouts, power conversion components and inter connecting bus-works. These standards will in turn enable the following [7]: technology insertion and upgrades via standard interfaces, reduced maintenance via "plug and play" modules, reduced cost due to increased product development efficiencies, reduced time to market, reduced commissioning costs, reduced design and development risks, and increased competition in critical technologies. PEBB implementation is the enabling technology for the IPS architecture desired for future combatants to allow a more robust and survivable system due to increased power source redundancy and multi-path power supply for all loads (Fig. 5) [8]. The advent of more reliable electronic power conversion components, in the form of PEBBs, makes the electric ship possible today.

Critical technologies required to enable the electric ship are:

- Improved energy storage devices (batteries, fuel cells, flywheels, super-capacitors, etc.)
- High power density propulsion motors, and
- High fidelity and high power conversion modules.

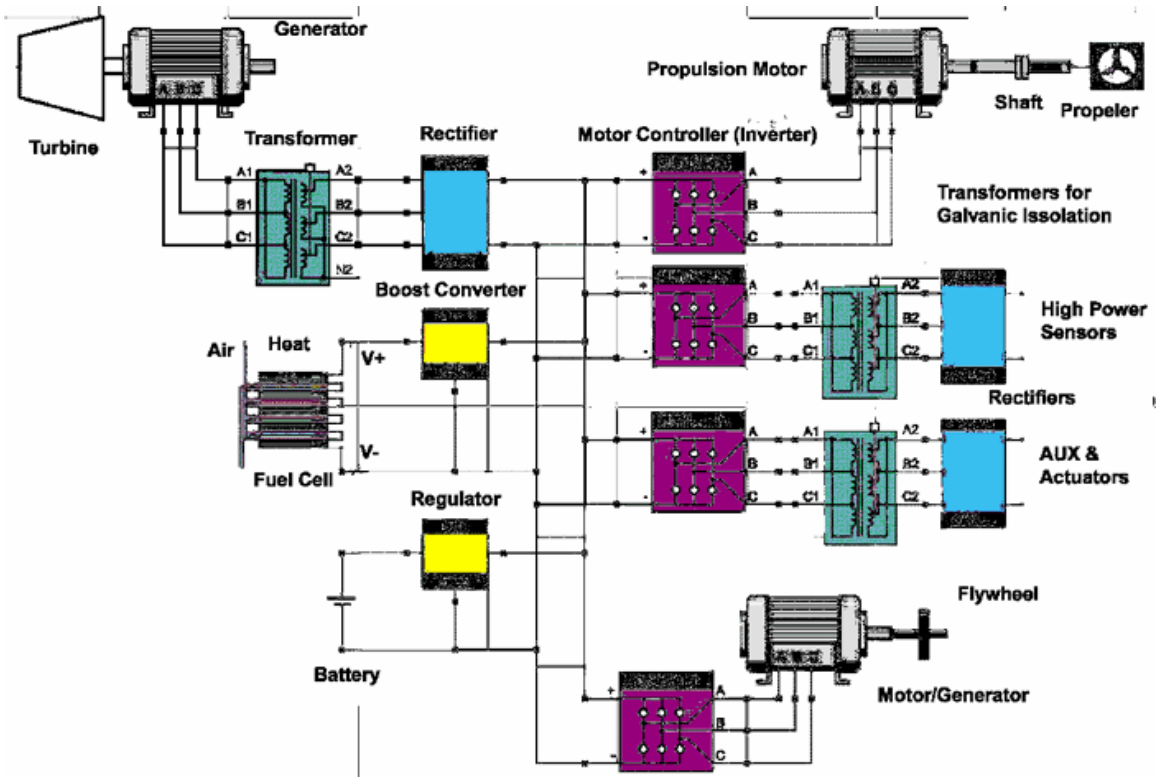

Figure 5. Advanced Electric Propulsion System [From Ref 8]

The commercial sector is driving the technology as the latest cargo vessel designs are built using IPS. The lure of vessel life-cycle savings (through savings in fuel consumption, manpower reduction, maintenance reduction, etc.) and increased platform time-on-task (or more precisely, less time in refit/overhaul) makes this new technology extremely attractive. From the Navy's perspective, the downside is that the pool of knowledge for legacy mechanical drive systems is becoming increasingly scarce and prohibitively expensive. The Navy not only finds itself needing IPS to enable the next-generation electromagnetic weapons systems and high power sensors, but it needs the technology to ensure that premier weapons platforms are affordable in the future. Ironically, the same motivations that drove ship designers to choose turbo-electric drive sixty years ago are forcing the same design decisions today. IPS will be the key that unlocks propulsion power for multi-Megawatt aircraft launch systems, weapons and sensors in an affordable way.

B. RESEARCH GOALS

This thesis will continue the research conducted previously on the hybrid inverter system [4, 5]. This inverter topology is a candidate to convert dc to the necessary ac power for a propulsion motor in the 40-50 MW range. The hybrid system investigated consists of a bulk six-step (180°) voltage-source inverter (VSI) and a high-fidelity hysteresis controlled current-source inverter (CSI) which acts as an active filter for the bulk inverter. The goals of this thesis are to:

- Simplify the six-step inverter controller design for the VSI. Provide variable operational frequency capability.
- Modify the Hysteresis controller to provide a control signal delay. This allows the IGBT driver cards to power up before they receive gating signals.
- Design a circuit to extract a reference sine wave which is phase-locked to the system output frequency. Ultimately this design will allow variable frequency operation of the system.
- Utilize commercially available Semikron PEBB as the power section for both the VSI and the CSI.
- Develop equations and optimize hysteresis bandwidth to produce the best (highest quality) output current in order to meet or exceed IEEE Standard 519 (1999) requirements for three-phase half-bridge inverters. Total Harmonic Distortion (THD) of 2.5% or better desired.
- Model the system using SIMULINK to provide proof of concept.
- Couple the bulk six-step inverter and the hysteresis controlled inverter to create a hybrid parallel inverter system.
- Test the hybrid system to determine the optimal operating set-point. Increase the power output of the system.

Successful testing of the improved hybrid hysteresis inverter will validate the efficacy of the system for use in powering small and medium sized motor loads.

C. APPROACH

Both inverters used in References 9 and 10 were replaced with commercially available 20 kVA Semikron IGBT PEBBs. They have three half-bridges rated at 50A/1200V and an IGBT/diode brake for protection. The unit is able to produce its own dc bus using an installed, uncontrollable three-phase diode rectifier module. The Semikron SKHI 22B drivers were used to gate the half-bridges. The bulk controller was replaced with a shift register driven six-state machine. The bulk inverter currents for all three phases were measured using Hall-effect sensors and passed through a low-pass filter and a phase correcting all-pass filter to create the hysteresis reference waveforms. These waveforms were passed to the modified hysteresis controller based on the circuit constructed in Reference 9. Finally the hybrid inverter was constructed and tested to determine the operational efficacy of the new layout and redesigned controllers.

D. THESIS ORGANIZATION

Chapter I is an overview of the research effort and the layout of the thesis.

Chapter II is a brief overview of the theory behind the designed components and a review of the mathematical theory behind the various hybrid inverter components. Significant areas covered are: half-bridge inverter theory, six-step controller theory, hysteresis controller theory, and the hybrid inverter theory.

Chapter III presents the design and construction of the Parallel Connected Hybrid Inverter bulk six-step and hysteresis controllers. Specific circuit designs covered are: bulk-six-step controller, Hall-effect sensor circuit, hysteresis controller filter circuit, and the modified hysteresis circuit.

Chapter IV presents the computer model and the simulation results

Chapter V chronicles the experimental results from the lab built prototype. Circuit performance measures and limitations are provided and areas of improvement are listed to assist in future research efforts.

Chapter VI provides conclusions, lessons learned, future research opportunities, and potential military applications.

The appendices provide pertinent computer code, circuit design calculations, relevant circuit schematics, and net lists for the circuits constructed in this lab.

II. BACKGROUND INFORMATION

A. OVERVIEW

This chapter provides background information on the major concepts explored in this research effort. Specific topics of significance are: the ac drive system, the chosen three-phase inverter topology, the bulk six-step controlled VSI, the hysteresis controlled CSI, and parallel-connected hybrid inverters.

B. AC DRIVE SYSTEM

A representative ac drive system consists of three sections: ac-to-dc rectification, energy storage, and dc-to-ac conversion (Fig. 6). A three-phase power generation device provides poly-phase ac power which is conditioned using ac-line filters and is provided to a rectifier unit to convert it into dc power. Figure 6 shows a 6-pulse controlled rectifier which will produce dc power with some harmonic content. These harmonics can be removed using a 2-pole filter and a capacitor bank to damp the harmonic oscillations. By using higher pulse count (12-pulse or 24-pulse) rectifiers, the dc output has lower THD and requires less filtering. SCR controlled-switch rectifiers allow the firing angle of the devices to be adjusted to match the load to improve the fidelity of the dc output again reducing the THD by dynamically matching the load.

The dc bus can be augmented by battery banks, fuel cell stacks, solar cells, or other energy storage devices. The dc power is then converted back into a symmetrical ac output voltage of desired magnitude and frequency by the inverters, where it is delivered to the load.

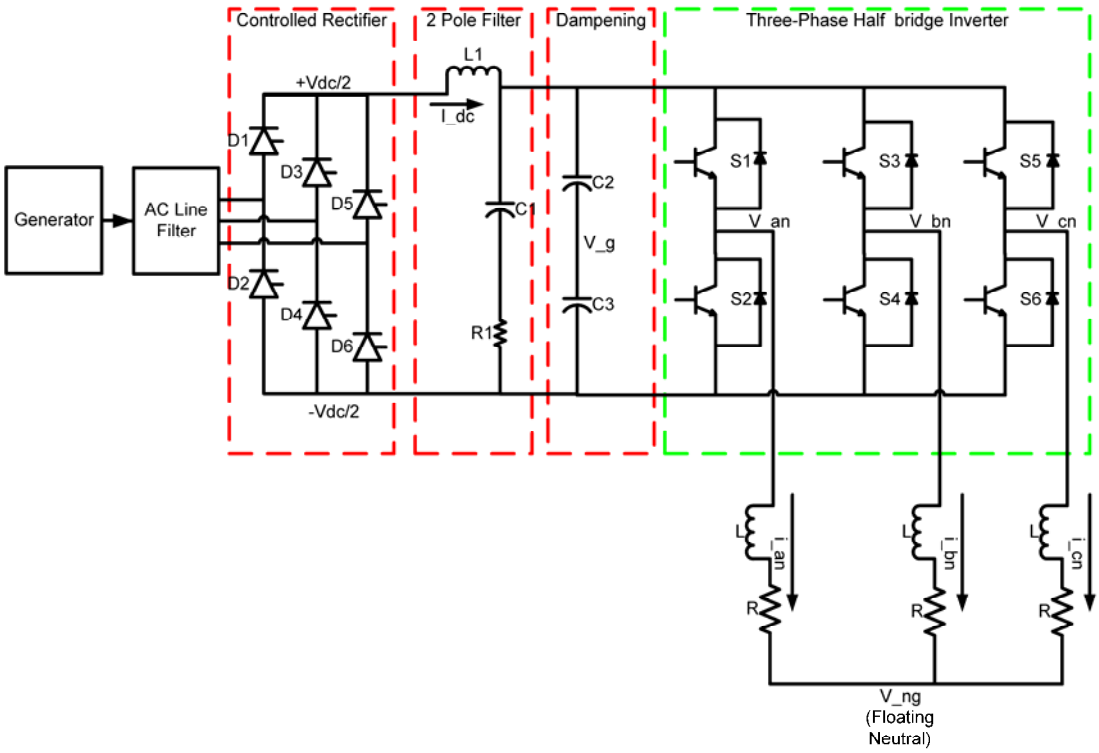

Figure 6. Three-Phase Inverter Powered RL Load [After Ref. 7]

C. THREE-PHASE BRIDGE INVERTER TOPOLOGY

The basic electronic building block for any inverter is the half-bridge (Fig. 7).

Half-Bridge Inverter

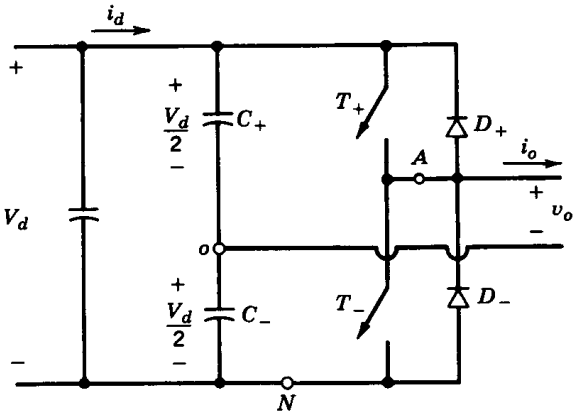

Figure 8-10 Half-bridge inverter.

• Capacitors provide the mid-point

Figure 7. Half-Bridge Inverter Topology [From Ref. 11]

A half-bridge consists of two controllable switches that transform the dc source into a quasi-ac output due to the switching action of the two switches. Across each half-bridge switch is a diode, placed in the reverse direction of the transistor current, to provide a free-wheeling path for inductive loads during switching transition. Additionally, two equal valued capacitors are connected in series across the dc voltage source with their junction located at the mid-potential point. The capacitors are sufficiently large, and the switching pattern is symmetrical, to keep the midpoint essentially constant (near ground in a floating system) with respect to both dc bus rails. Both switches (upper and lower) are never simultaneously ‘on’. Such an event would cause a ‘shoot-through’ condition, potentially destroying the switches [11].

The fully controllable switches in the inverter should ideally display the following characteristics [11]:

- Block large forward and reverse voltages with zero current leakage when switched off
- Conduct large currents (in one direction only) with zero voltage drop when switched on
- Switch from the on state to the off state (and vice versa) instantaneously when gated
- Display vanishingly small power requirements from control source to gate the switch

In practice, there is a minute time period when the switch is transitioning from the on-state to the off-state where both a voltage drop and current flow exist. Figure 8 illustrates a worse case scenario when a switching transient experiences near maximum values for both current and voltage. Actual device switching losses are present at a fraction of the worse case power loss. As the switching frequency increases and more transition states occur over a set time period there is a corresponding increase in the power loss of the switch [11]. This in effect lowers the power rating of the switch at higher switching frequency operation. Furthermore, in order to reduce the chance of inadvertent power losses, none of the semiconductor switches are ever intentionally operated in their active regions; they are either in the saturation region (on) or in the cut-off region (off) [12]. If the switch were to operate in the active region there would be a significant amount of power lost in the switch as a voltage drop and current flow would both exist in the device.

Switching Characteristics (linearized)

Switching Power Loss is proportional to:
- switching frequency
- turn-on and turn-off times

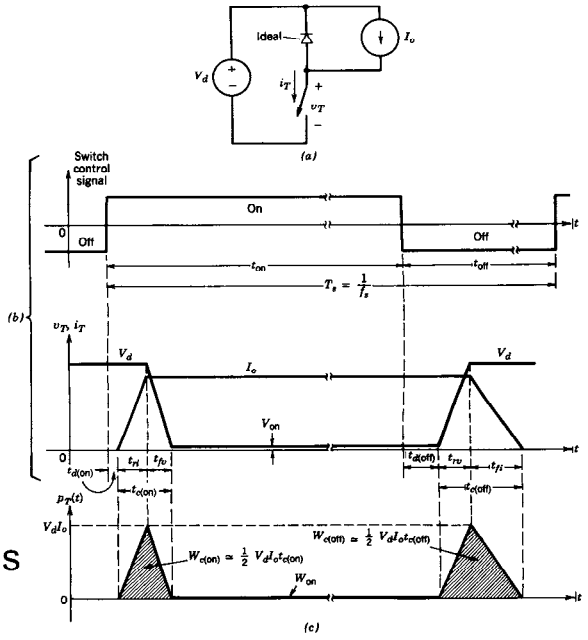

Figure 2-6 Generic-switch switching characteristics (linearized): (*a*) simplified clamped-inductive-switching circuit, (*b*) switch waveforms, (*c*) instantaneous switch power loss.

Figure 8. Worst Case Power Loss Across a Switch [From Ref. 11]

The choice of device to use as a switch is driven by the power required by the system and the switching speed required. MOSFET devices are easily controlled and are ideal for low power applications at higher switching frequencies. For electric drive applications they are unsuited for the high power outputs required. A comparison of the various power electronic devices available for medium to high power inverters is provided in Table 2. Practical fully controllable switches of interest to the Navy include the Insulated Gate Bipolar Transistor (IGBT), the Injection Enhanced Gate Transistor (IEGT), the Gate Turn-Off thyristor (GTO) and the Integrated Gate Commutated Thyristor (IGCT).

The IGBT has become dominant in the power conversion industry and provides the best compromise between output power available and switching frequency. IGBTs do not have a blocking capability in the reverse direction which necessitates the use of a reversed-biased blocking diode placed in series but they do not require costly snubber circuits to operate. They are generally packaged in a half-bridge module to integrate electrical insulation and heating removal from the switches. Since its introduction into the

marketplace in the mid 1980's, the IGBT has improved from a low-power device to a medium power one rated at up to 4500V and/or 1200A. IGBTs can be used for high power applications but they require series-connected multi-level topologies driven by complex controller strategies [11]. The next generation IGBT, the Injection Enhanced Gate Transistor (IEGT), has a very low on-state voltage and lower projected power losses than thyristor based devices. It has projected ratings of up to 4500 Volts and 4000 Amps and maintains the high switching speed of the IGBT. Devices rated at 6500 Volts are expected in the next few years [14]. The operational limits of the IEGT are approaching the ability to allow solid state conversion in the US market where 4150V systems are prevalent [13].

DEVICE:	GTO	IGCT	IGBT	IEGT
Device Type	Thyristor Based Devices		Transistor Based Devices	
Efficiency	Low	Medium-High	High	High
Gate Control Signal	Current	Current	Voltage	Voltage
Gate Current	400-1000A	4000A	< 1A	< 1.5 A
Voltage Rating	High	6000V	4500V	4500V
AC Voltage Limit (2/3 Voltage Rating)	High	4000 V	3000 V	3000 V
Current Rating	1000A	4500A	1200A	4000A
Switching Losses	High	Medium	Low	Low
Snubber Parts	Many	None	None	Low
Switching Speed	Low	Medium	High	High

Table 2. Power Device Comparison [Refs. 13 and 14]

GTOs have the slowest rated device switching times but provide the highest power out capability. They are the best choice for extremely high power applications. The trade-off in their use is the complexity of the gate driver circuitry required and the

snubber circuit necessary to effectively use it. Designed to have both gate-controlled turn-on and turn-off capability, the GTO turns-on in a fully conducting mode with a low forward voltage drop, and turns-off when a turn-off pulse is applied to the gate. Snubber circuits are designed to prevent three things: full current from going through the device until the device is fully on, large over-voltages during turn-off (and reduce voltage changes that may retrigger the device), and alter the switching waveforms to minimize the chance of full voltage and full current at the same time in the device. Snubbers generally add to the complexity and the cost of the switch control and protection circuitry. Next generation thyristor-type devices provide the high power output without the associated bulky gate drivers, slow turn-off, and costly snubbers. The IGCT is basically a GTO with hard turn off and high gate power requirement to switch [11]. IGCTs do not require snubbers and display lower on-state losses than the GTO. Thyristor based devices are disadvantageous in that they require large current impulses to trigger them which equates to a larger, albeit momentary, power losses in the system.

For poly-phase systems the half-bridge count will equal the number of phases. This is the topology of the Semikron IGBT-based prototype PEBB used in this thesis to demonstrate the parallel connected hybrid inverters. The three-phase bridge inverter consists of three half-bridges connected in parallel (Fig. 9) and a chop transistor and diode pair. This feature will not be used. The dc-ac inverter receives conditioned dc power (V_{dc}) produced by an uncontrolled diode bridge rectifier. This input is applied across the two in-series 1100 micro Farad damping capacitors (labeled C1 and C2) which help provide the stabilized mid-potential point. Note the numbering of the six controllable switches, labeled S1-S6. This numbering sequence shall be followed throughout this thesis.

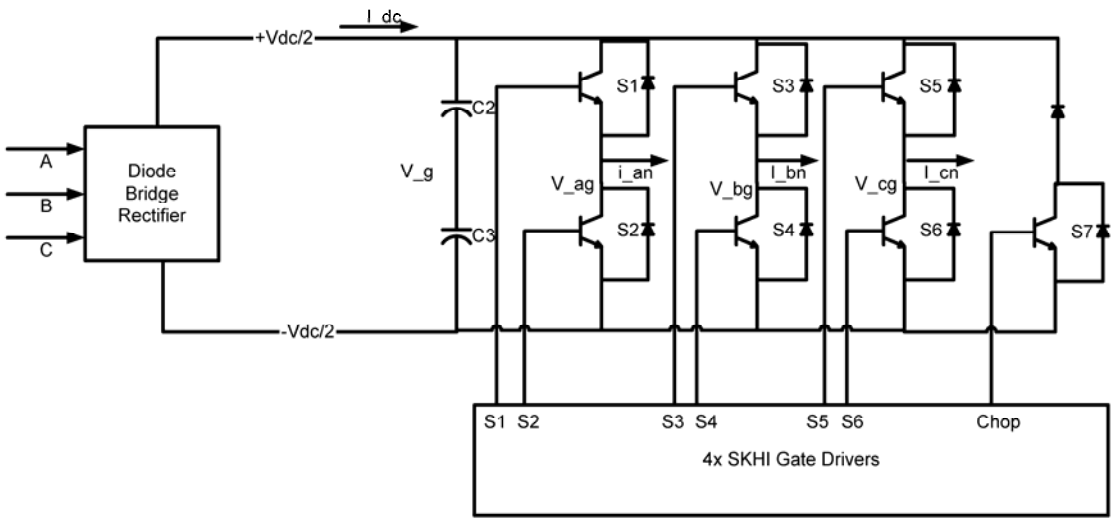

Figure 9. Semikron PEBB

D. SIX-STEP CONTROLLED VOLTAGE-SOURCE INVERTER

One of the simplest switching control methods used to trigger the switches in the three-phase bridge inverter is the six-step switching scheme (also called 180° voltage-source operation or square-wave switching). In this scheme each switch in the inverter is on for one-half cycle (180°) of the desired output frequency [11]. The switches (Fig. 10) follow a three-phase cyclic pattern as shown in Table 3. There is a switching event every 60° for the six-step controller strategy as illustrated in Figure 11.

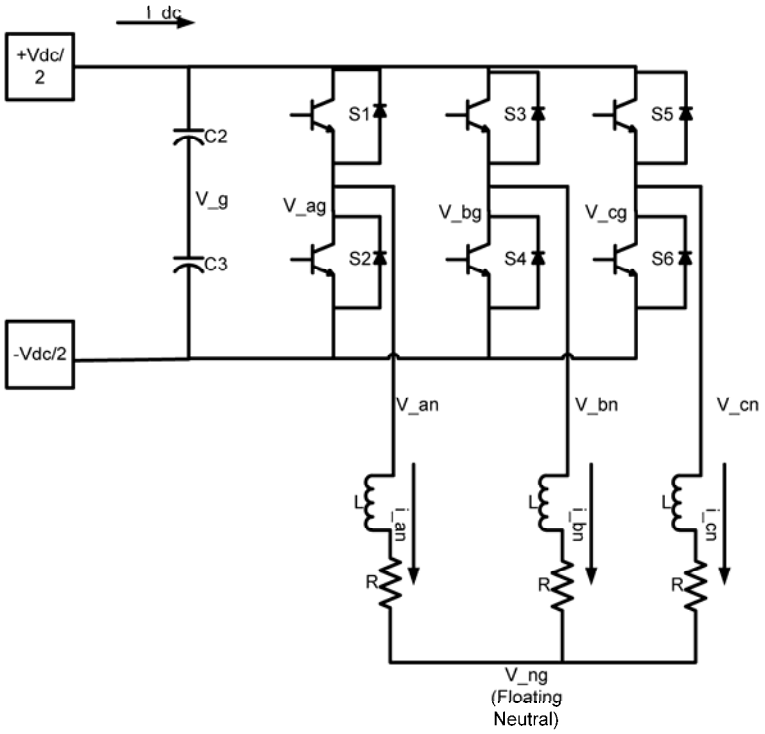

Figure 10. Three-Phase Bridge Inverter [After Ref. 12]

Wave portion	Interval	Switches Closed	Gate Signals
Positive Half	0° to 60°	T1 closed at 0°	S1-S4-S5
Negative Half	60° to 120°	T6 closed 180° after T5	S1-S4-S6
Positive Half	120° to 180°	T3 closed 120° after T1	S1-S3-S6
Negative Half	180° to 240°	T2 closed 180° after T1	S2-S3-S6
Positive Half	240° to 300°	T5 closed 120° after T3	S2-S3-S5
Negative Half	300° to 360°	T4 closed 180° after T3	S2-S4-S5

Table 3. Six-step Inverter Three-phase Cyclic Switching Pattern

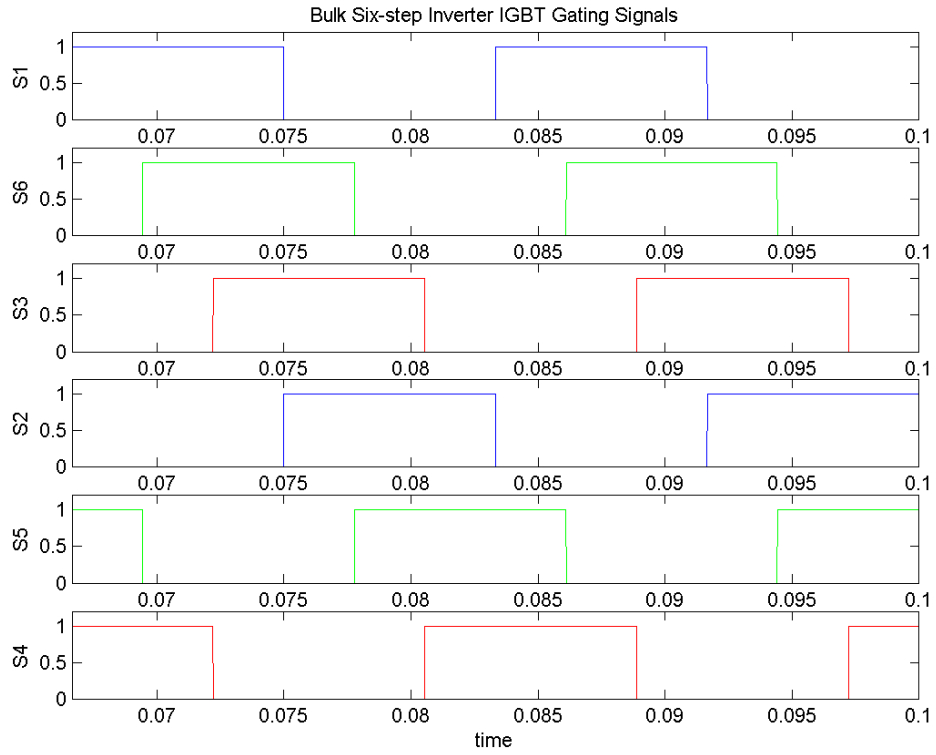

Figure 11. Six-Step Inverter Gate Control Signals (f_c = 60 Hz)

V_{dc} =100 V	INTERVAL					
VOLTAGE	0°-60°	60°-120°	120°-180°	180°-240°	240°-300°	300°-360°
V_{an}	$\frac{1}{3}V_{dc}$	$\frac{2}{3}V_{dc}$	$\frac{1}{3}V_{dc}$	$-\frac{1}{3}V_{dc}$	$-\frac{2}{3}V_{dc}$	$-\frac{1}{3}V_{dc}$
V_{bn}	$-\frac{2}{3}V_{dc}$	$-\frac{1}{3}V_{dc}$	$\frac{1}{3}V_{dc}$	$\frac{2}{3}V_{dc}$	$\frac{1}{3}V_{dc}$	$-\frac{1}{3}V_{dc}$
V_{cn}	$\frac{1}{3}V_{dc}$	$-\frac{1}{3}V_{dc}$	$-\frac{2}{3}V_{dc}$	$-\frac{1}{3}V_{dc}$	$\frac{1}{3}V_{dc}$	$\frac{2}{3}V_{dc}$
V_{ab}	V_{dc}	V_{dc}	0	$-V_{dc}$	$-V_{dc}$	0
V_{bc}	$-V_{dc}$	0	V_{dc}	V_{dc}	0	$-V_{dc}$
V_{ca}	0	$-V_{dc}$	$-V_{dc}$	0	V_{dc}	V_{dc}

Table 4. Line-to-Neutral and Line-to-Line Voltages for the Six-step Inverter [After Ref 11]

The resultant output line-to-line voltages and line-to-neutral voltages are provided in Table 4 and illustrated in Figures 12 and 13. The line-to-neutral voltages demonstrate that the three-phase switching scheme provides a more sinusoidal output than one full-bridge square-wave inverter alone.

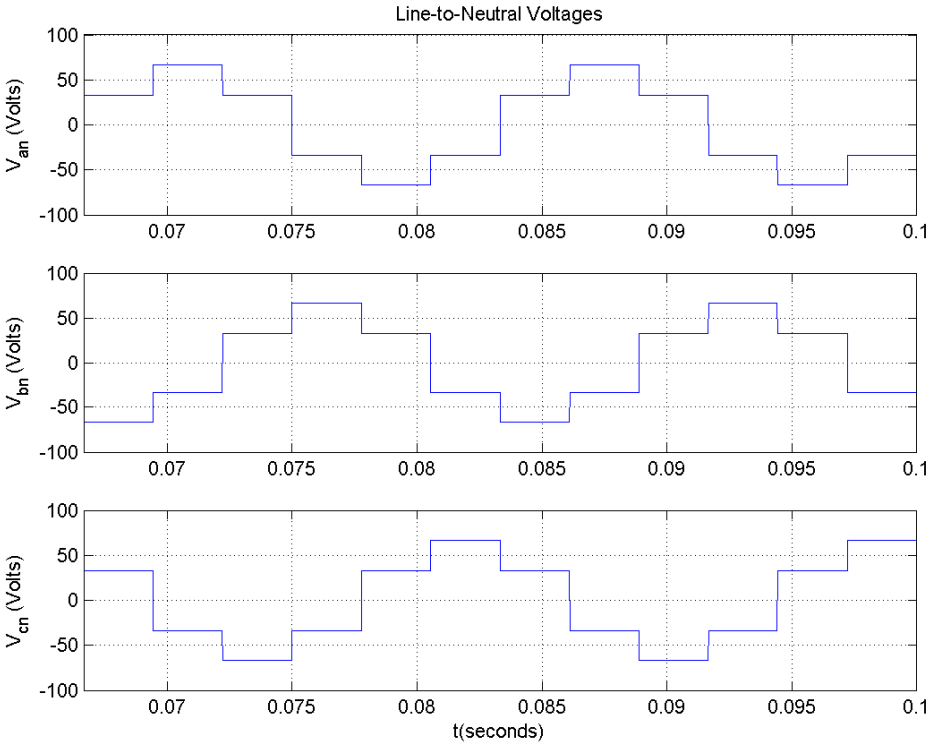

Figure 12. Six-step Inverter Line-to-Neutral Voltages

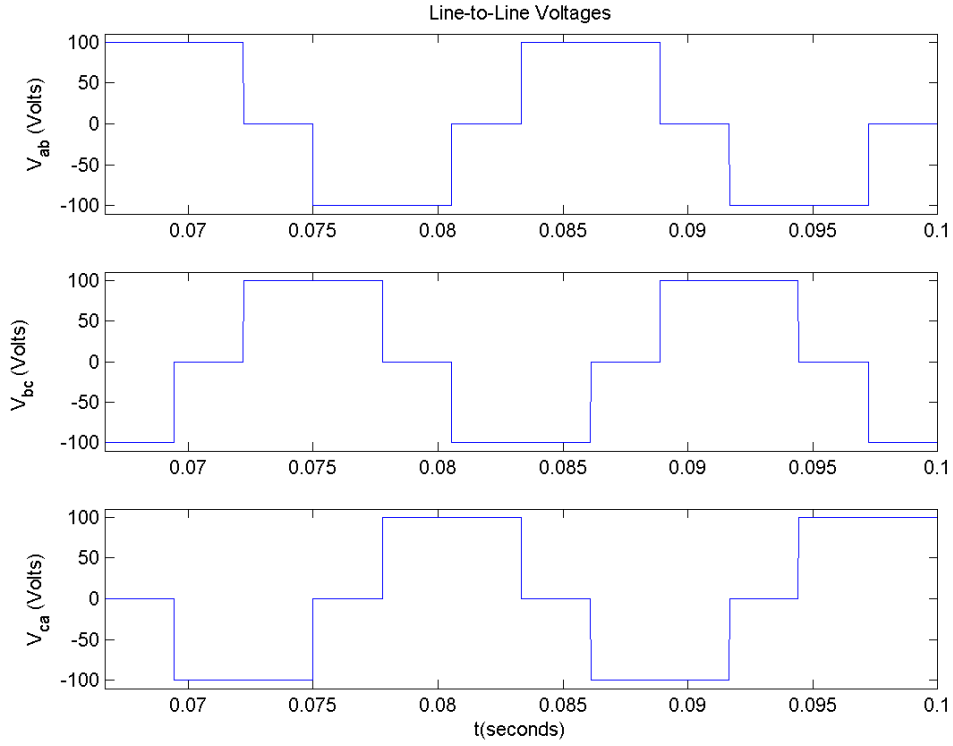

Figure 13. Six-step Inverter Line-to-Line Voltages

The line-to-neutral voltage, V_{an}, may be represented by the Fourier series [12]:

$$V_{an} = \frac{2}{\pi} V_{dc} \cos(\theta_c) + \frac{2}{\pi} V_{dc} \sum_{k=1}^{\infty} \left(\frac{(-1)^{k+1}}{6k-1} \right) \cos((6k-1)\theta_c) + \left(\frac{(-1)^{k}}{6k+1} \right) \cos((6k+1)\theta_c) \qquad (2.1)$$

where V_{dc} is the dc bus voltage, and θ_c is the converter angle. The line-to-neutral current, I_{an}, can be calculated for each harmonic value of V_{an} by the following equation:

$$I_{an} = \frac{V_{an}}{|Z|} \qquad (2.2)$$

where Z is the complex ac load impedance for each harmonic frequency. Z is given by:

$$|Z| = \sqrt{R + jk\omega L} \qquad (2.3)$$

where R is the load resistance, L is the load inductance, and k is the harmonic.

Figure 14 shows the first twenty-one harmonics of I_{an} obtained by these equations. All even harmonics are non-existent and the all odd harmonics which are multiples of three are suppressed. The effect of these harmonics on the current waveform is shown in Figure 15. Because of the harmonic content, the power delivered to the three-phase load is not constant. This implies that the power into the converter and hence the dc current into the converter is not constant [12].

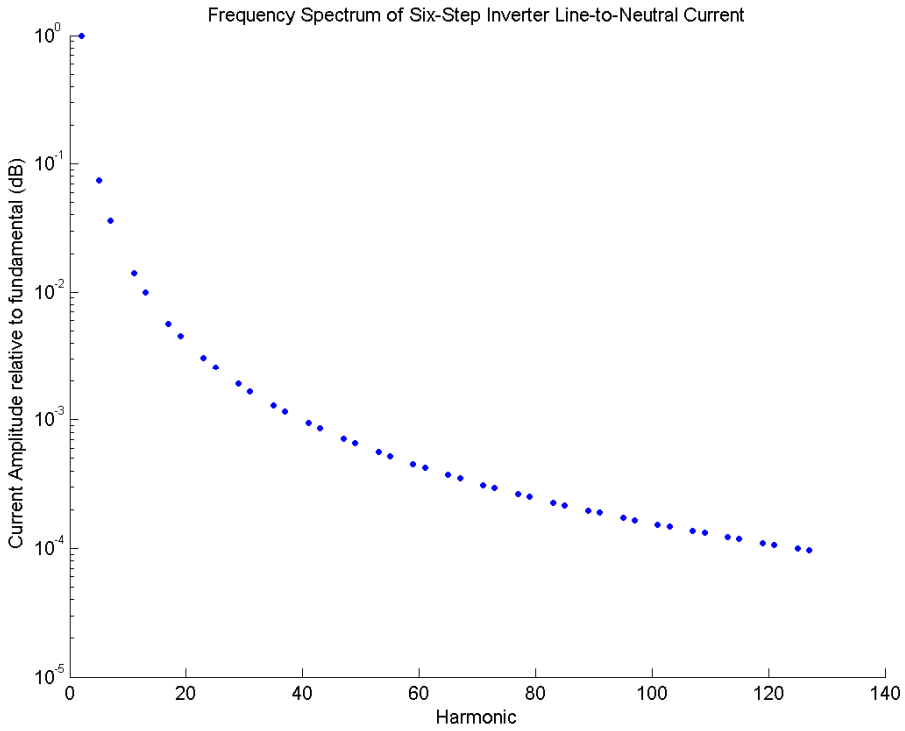

Figure 14. Six-step Inverter Line-to-Neutral Current Harmonics

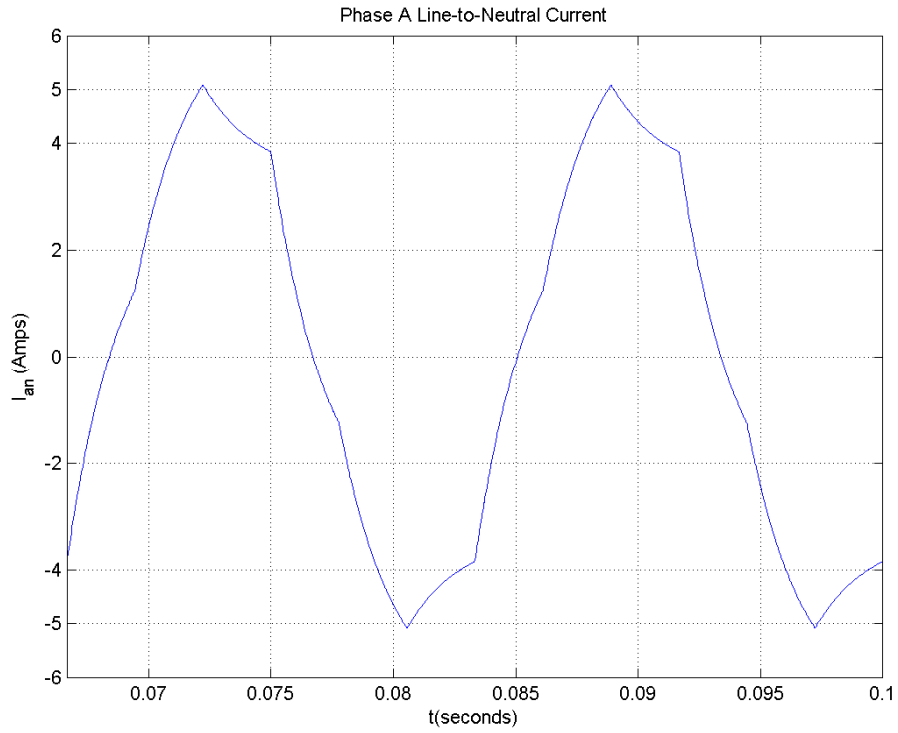

Figure 15. Phase A Line-to-Neutral Current

THD is given by [11]:

$$\text{THD} = 100 \times \sqrt{\sum_{k \neq 1}^{\infty} \frac{(I_k)^2}{(I_1)^2}}\,. \tag{2.4}$$

A numerical analysis of the six-step inverter current THD versus displacement power factor illustrates that for a purely inductive load (DPF nearly zero) the THD will be 5.67%. For a purely resistive load (DPF = 1) the THD will be 28.43%. A 0.8 DPF correlates with a current THD for the system of about 9.03% (Fig. 16). Figure 16 demonstrates the relationship between DPF and THD for a 60 Hz system where the system impedance is unity and the resistance is equal to the DPF. The tabulated results used to create this plot are provided in Appendix B. Using the experimental inductive load of DPF = 0.763 at 60 Hz, the calculated theoretical value of the current THD for the bulk inverter is 8.46% which is on the curve.

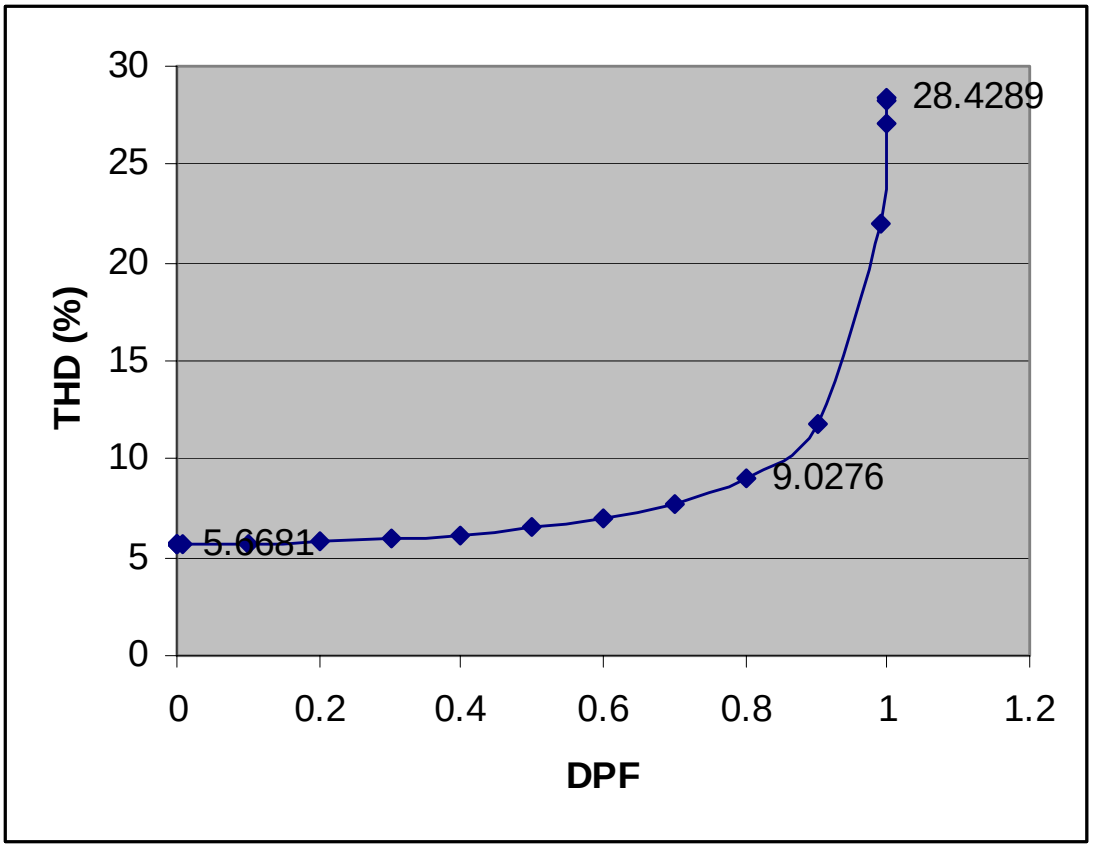

Figure 16. Current THD (%) versus Load DPF

The principal advantage of using the six-step control method is the simplicity of control strategy. The frequency of the output can be varied by simply changing the controller frequency which times the gate signals. Another advantage is that the amplitude of the fundamental generated with the six-step inverter is the largest value that can be obtained using the three-phase bridge inverter topology [12].

One disadvantage of this control strategy is that there is considerable harmonic content in the output which can significantly lower circuit efficiency. This manifests itself as torque pulsations in motors, tripped circuit breakers, flickering lighting and overheating in magnetic windings due to high frequency core losses which contribute to the net system efficiency loss. Another disadvantage is that the amplitude of the output can only be controlled by adjusting the amplitude of the dc source.

E. HYSTERESIS CONTROLLED CURRENT-SOURCE INVERTER

A hysteresis controlled CSI converts a dc voltage source into an ac current source. The controller is a direct large-signal device that utilizes upper and lower limits to direct switching signals. The switching boundaries are defined in terms of only one of the system's state space variables: the inductive current. The load current is controlled within a narrow tolerance band ($2\times\Delta_h$) based on a given sinusoidal reference value (I_{ref}) for each phase. The hysteresis controller takes (I_{ref}) and adds a small error tolerance, a preset deviation (Δ_h), to it to generate the upper limit. The lower limit is generated by subtracting Δ_h from I_{ref}. The output current (I_o) is then compared to this tolerance band (Fig. 17) [12].

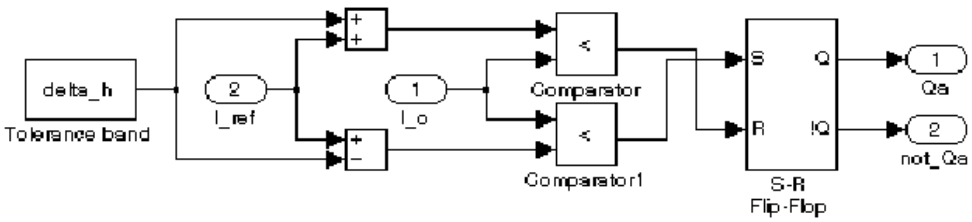

Figure 17. Hysteresis Controller (showing one phase only)

Because only one state variable is used and both upper and lower limits are specified, dead-band space is provided between the two bands to ensure that 'chatter' (infinite switching speed) does not occur. If the output tries to go above the upper bound then the controller switches the lower switch in the bridge on to apply the negative rail voltage of the dc bus and drive the current back into the band. If the output tries to go below the lower bound the controller switches the upper switch in the bridge on to apply the positive rail of the dc bus and drive the current upward back into the band. If the output is within both boundaries the switch positions (upper and lower) remain unchanged (Fig. 18) [11, 12].

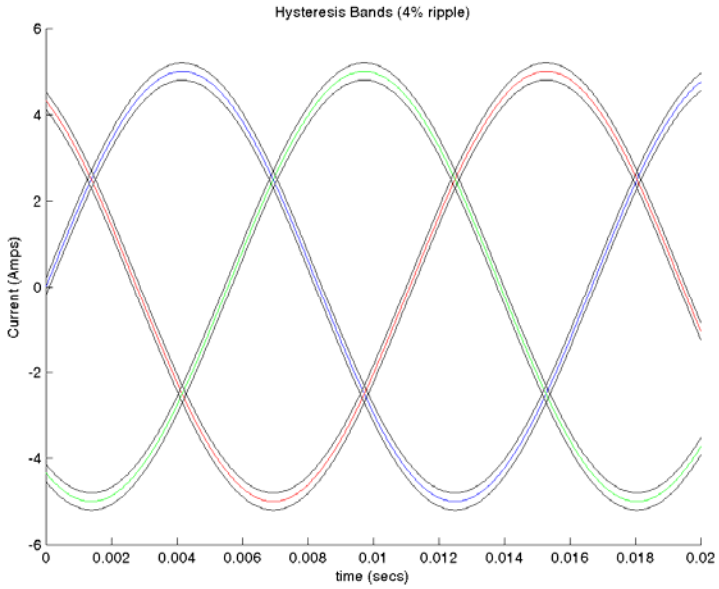

Figure 18. Hysteresis Bands (4% ripple)

Table 5 demonstrates the logic behind the hysteresis controller for each of the three-phases and switching states of the bridge inverter switches.

LOGIC	SWITCH	SWITCH POSITIONS
$i_{oa} \leq i_{refa} - \Delta_h$	Set $V_{ag} = \frac{V_{dc}}{2}$	T1 is ON and T2 is OFF
$i_{refa} - \Delta_h \leq i_{oa} \leq i_{refa} + \Delta_h$	No Change	Unchanged
$i_{oa} \geq i_{refa} + \Delta_h$	Set $V_{ag} = \frac{-V_{dc}}{2}$	T2 is ON and T1 is OFF
$i_{ob} \leq i_{refb} - \Delta_h$	Set $V_{bg} = \frac{V_{dc}}{2}$	T3 is ON and T4 is OFF
$i_{refb} - \Delta_h \leq i_{ob} \leq i_{refb} + \Delta_h$	No Change	Unchanged
$i_{ob} \geq i_{refb} + \Delta_h$	Set $V_{bg} = \frac{-V_{dc}}{2}$	T4 is ON and T3 is OFF
$i_{oc} \leq i_{refc} - \Delta_h$	Set $V_{cg} = \frac{V_{dc}}{2}$	T5 is ON and T6 is OFF
$i_{refc} - \Delta_h \leq i_{oc} \leq i_{refc} + \Delta_h$	No Change	Unchanged
$i_{oc} \geq i_{refc} + \Delta_h$	Set $V_{cg} = \frac{-V_{dc}}{2}$	T6 is ON and T5 is OFF

Table 5. Hysteresis Controller Logic

The instantaneous single phase switching frequency can be predicted by using the following equation (derivation of this equation is presented in Appendix B):

$$f_s = \frac{V_{dc}^2 - 4R^2\left(I_{max}^2 - I_{refa}^2\right)}{8L_t\Delta_h V_{dc}}, \tag{2.5}$$

where, V_{dc} is the dc bus voltage, I_{max} is the maximum reference current amplitude, I_{refa} is the reference current signal, L_t is the load inductance, and Δ_h is the constant valued offset used to create the tolerance band. The reference offset (Δ_h) is exactly one-half of the tolerance bandwidth.

Equation (2.5) accounts for the four factors that determine the hysteresis switching frequency: dc bus voltage, back emf, load inductance, and tolerance bandwidth. The switching frequency will be the fastest when the reference current reaches a maxima or minima value and will be the slowest when the reference is zero. A larger resistive load will result in a larger switching frequency. A larger load inductance will result in a slower switching frequency. The inductance cannot be zero or the switching frequency will become infinite. The operating frequency of the hysteresis controller is variable and is inversely proportional to the width of the hysteresis band. This determines how fast the current changes from the upper band to the lower band and vice versa. Finally, the frequency varies directly with the difference of I_{max} and I_{refa}. When the difference is zero the frequency is the highest, when it is equal to I_{max}, the frequency is the lowest. The maximum frequency occurred when I_{refa} was at a maxima or a minima and the minimum when I_{refa} equaled zero as demonstrated experimentally (Fig. 19) [9, 10].

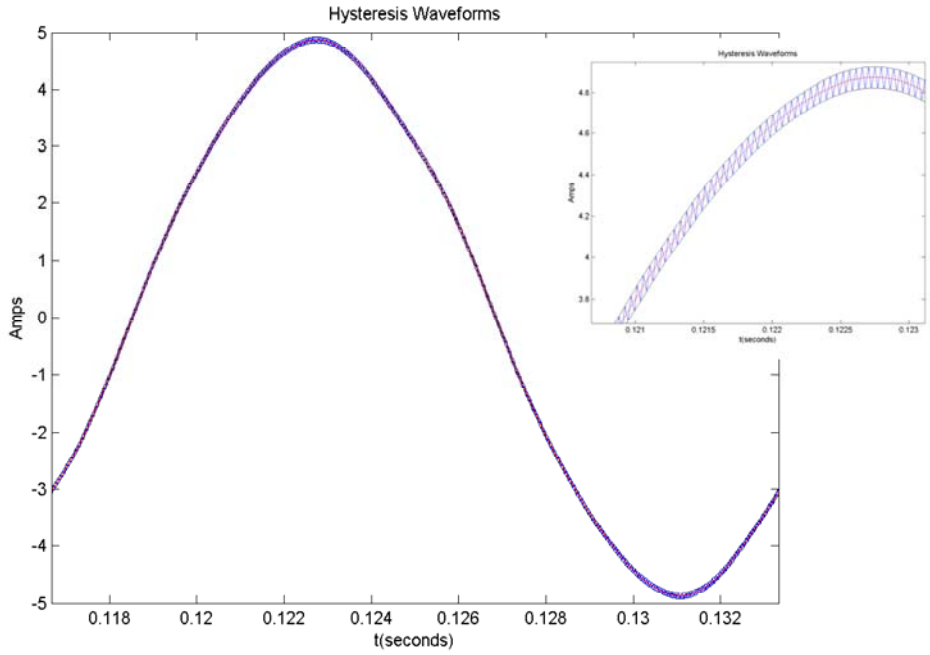

Figure 19. Hysteresis Single Phase Switching

This frequency relationship is only valid for single phase operation. For polyphase hysteresis control an additional relationship exists between the phase current response and the switching action of the other phases. Switching events in the other phases affect the observed phase's current which is not reflected in the equation. Equation 2.5 should, however, provide a good estimation of the switching frequency range expected. A 10% safety margin is added to the calculated single-phase maximum switching frequency ensure that the hysteresis controller does not ever surpass the maximum operational switching frequency of the PEBB which is 20 kHz.

The attraction of the hysteresis inverter is that it allows the load dynamics to be ignored; however, there are some significant limitations on this topology. The first is that there is a limit on the range of currents that can actually be commanded. The maximum peak line-to-neutral voltage that can be controlled is $\frac{2}{3}V_{dc}$. The peak line-to-neutral must be less than this value if the commanded current is to be obtained. The peak line-to-line voltage must be lower than the peak line-to-line voltage the converter can achieve, which

is identical to V_{dc}. This limit defines the steady-state range over which the currents can be expected to track and is more restrictive than the previously discussed limit [12].

F. PARALLEL CONNECTED HYBRID INVERTERS (PCHI)

In order to maximize system efficiency and to improve power supply reliability, a hybrid inverter topology with a hysteresis controlled CSI placed in parallel with a six-step controlled VSI. The VSI will produce the maximum amplitude voltage available with the three-phase bridge inverter topology and the CSI will produce purely harmonic output at the levels required to cancel the non-fundamental frequency harmonic content of the VSI output. The result will be a filtered output current that contains minimal harmonic content. The parallel inverter topology also improves system reliability by providing redundant power to the load to ensure that motive force is available in the event that one inverter fails [9].

Figure 20 is a system diagram of the paralleled hybrid inverter system studied in the previous thesis effort [10]. The resultant hybrid current THD of 3.2% was an improvement over the raw six-step VSI current THD. There are several drawbacks in this controller design. The bulk controller was inefficient and complicated. It required three sine waves to be generated which were then digitized using comparators to create the six gating signals. The Wein-bridge oscillator used to generate the system operating frequency was complex and was unable to be readily tuned to a new system operating frequency. Finally the bulk controller was not truly independent of the hysteresis controller.

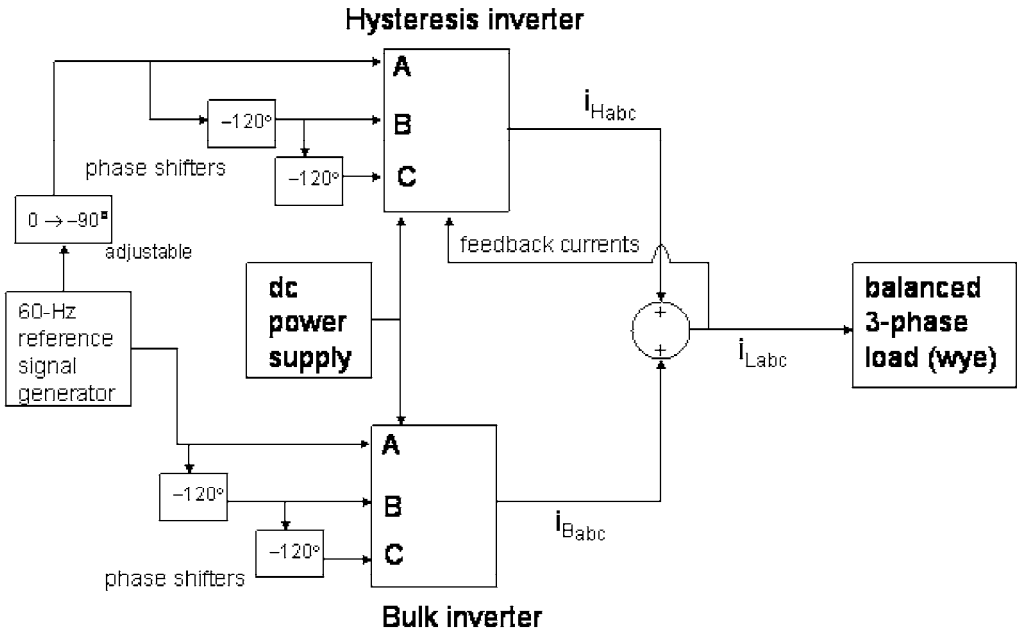

Figure 20. Parallel Connected Hybrid Inverter System [From Ref. 10]

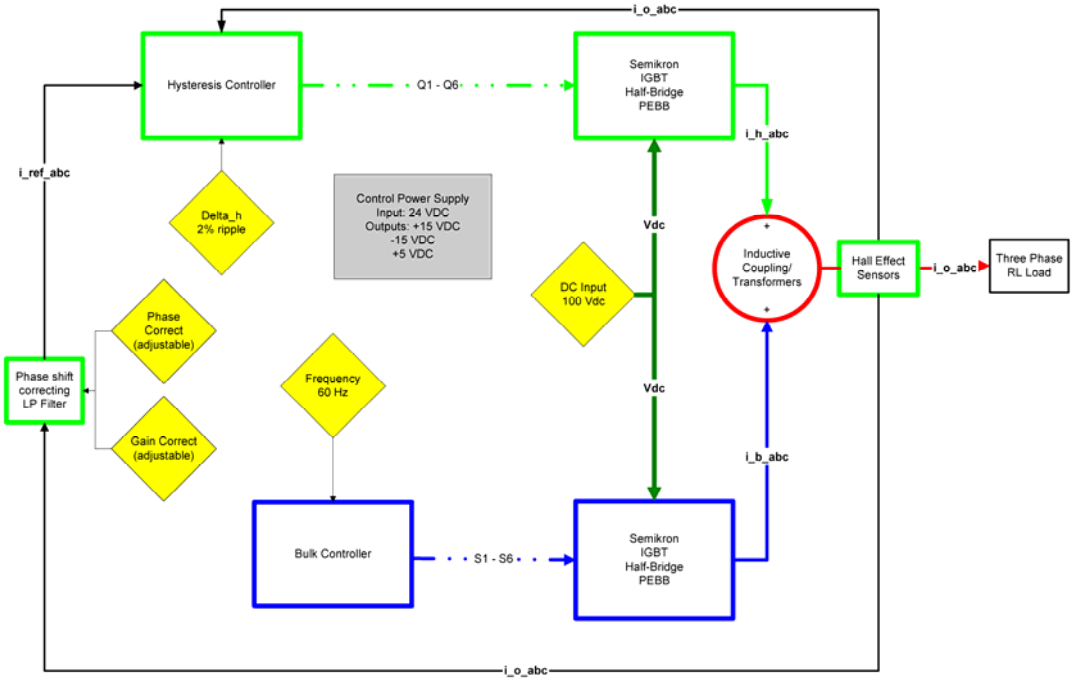

Figure 21. Revised Parallel-Connected Hybrid Inverter Control Strategy

For this thesis, a new control strategy will be used for the PCHI (Fig. 21). In this architecture the dc bus is set to operate at a prescribed voltage level and the six-step (bulk) inverter independently provides the frequency reference for the system. The bulk six-step VSI controller produces six gating signals; each offset sixty degrees from each other, which are sent to a PEBB in the correct sequence to switch the IGBTs on and off. This generates the initial three-phase ac output voltage and current for the load. The hysteresis controller senses the output current of each phase and filters the resultant signal, with a manually adjustable filter, to produce the reference sine waves. Ultimately the filter will be phase locked to the desired system frequency and will have an automatically adjustable gain correction to ensure that the reference signal is both phase matched and amplitude matched to the bulk inverter output current.

The hysteresis controller receives the reference signals and adjusts the reference by a preset tolerance amount. This produces the upper and lower limits for the tolerance band. The bandwidth is set to two percent of the output current amplitude. The hysteresis controller then compares the unfiltered output current to the phase reference sine waves to produce six gate control signals. If the output current for a phase is at the upper limit of the tolerance band the lower IGBT in the half-bridge is gated on to reduce the current. If the output current is at the lower limit then the upper IGBT is switched on to increase the current. The high fidelity hysteresis controlled PEBB will switch the IGBTs to produce an output which will cancel the harmonic content of the bulk six-step PEBB to create a nearly harmonic free three-phase output current. An added benefit of this strategy is that as the hysteresis-controlled CSI filters the output current, the reference waveform quality improves driving the system error to zero. The reference waveform is therefore conditioned twice; once by the filters and again by the hysteresis filtering of the load currents which results in a more finely tuned reference waveform.

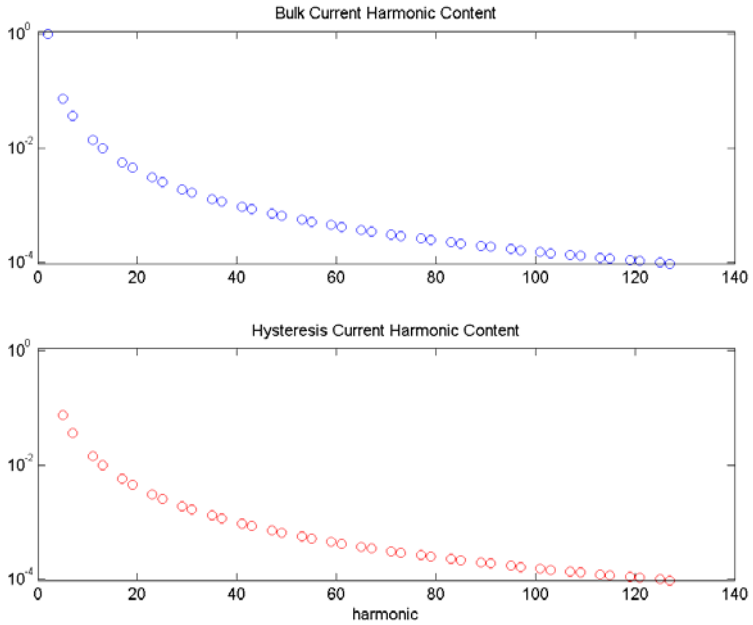

Figure 22. Inverter Harmonics Comparison

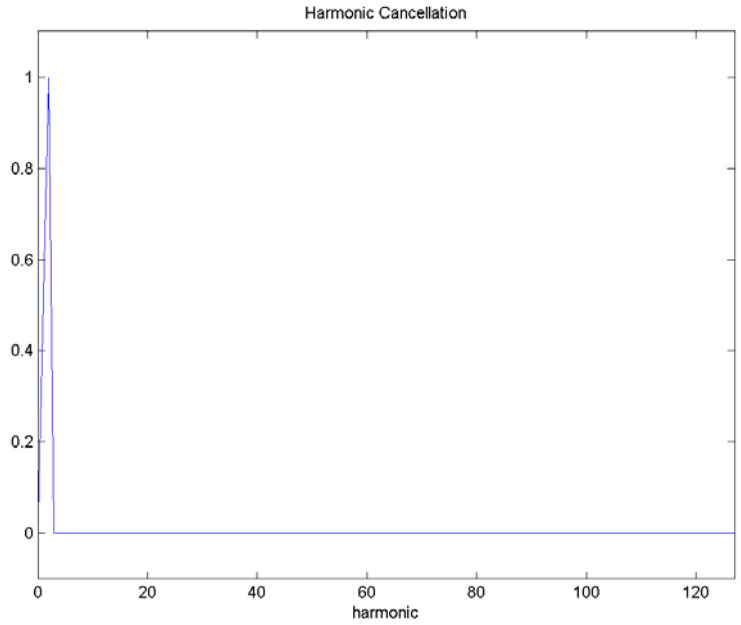

Figure 23. PCHI Harmonic Cancellation

The goal will be to have the hysteresis controlled inverter produce an output which will cancel the high harmonics of the six-step inverter while leaving the fundamental unaffected (Fig. 22). Thus the hysteresis inverter will act as an active filter and will cancel the harmonics present in equation 2.1, leaving only the fundamental component (Fig. 23). The outcomes of this improved control strategy are: to reduce the load current THD to 2.5% or better, to improve transient response time and, ultimately, to provide variable frequency operation.

G. SUMMARY

This chapter provided an overview of the major concepts that will be explored in this research effort. The next chapter will expand upon the foundation set to create a computer model and generate a circuit design to implement the hybrid parallel inverter control strategy and to create a low harmonic content current waveform.

III. HYBRID PARALLEL INVERTER CONTROLLER DESIGNS

A. OVERVIEW

To implement the improved control strategy discussed in the previous chapter, several circuits were designed and built in the lab. This chapter is a description of those circuits. Specific designs covered are the bulk six-step VSI controller and the hysteresis CSI controller. Circuit diagrams and parts-lists itemizing components used are provided in Appendix C.

The use of the Semikron PEBB (see Fig. 9) simplified the controller design by providing integrated safety features to protect the switch and the circuit from damage. The four SKHI-22A IGBT drivers provide galvanic isolation between the power circuit and the control circuit. The drivers provide "shoot-through" protection utilizing simultaneous control of both IGBTs in one phase-leg through logic and set on-state signal dead-times. This inhibits the control signal of the complimentary switch until the other switch in the phase leg is completely off. Other protective features include short circuit protection, power supply under-voltage protection, and thermal protection. The first two features provide an error signal and inhibit the control signals until the fault is cleared. There are sensors located in the heat sink which disable the PEBB before destructive temperatures occur in the unit. The brake chopper and the associated driver were not used for this research effort.

The drivers require $\pm 15 V_{dc}$ for power. This was provided to both PEBBs independent of the other control circuits to ensure that adequate power was available for switch control and protection. The control signals must be greater than 11.5 volts to turn-on a switch and less than 6.5 volts for turn off. The maximum operational switching frequency is 20 kHz. The required voltage to power the installed cooling fan is $208\, V_{ac}$.

B. SIX-STEP CONTROLLER DESIGN

The bulk controller was completely redesigned for this thesis. The controller designed in Reference 10 was complicated and difficult to tune. The system frequency could not readily be changed once it was set. Instead of digitizing three sine-wave references to generate the six gate signals, a digital six-state token ring counter was used to generate six signals every one-sixth of a period. A block diagram of the controller is shown below (Fig. 24).

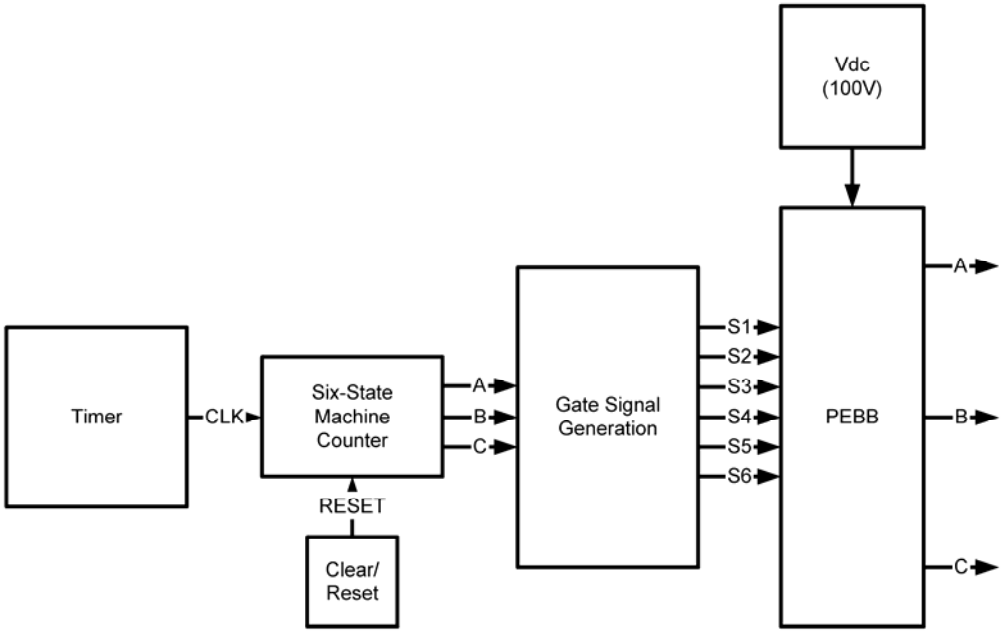

Figure 24. Bulk Six-step Controller Block Diagram

The controller is powered by 24Vdc. The necessary $15V_{dc}$ and $5V_{dc}$ levels required to power the ICs were generated using one LM7805 chip and one LM7815 chip. Both chips were installed using the circuit recommended in the datasheet.

The VSI controller was built around a simple sequential-logic six-state machine: the three-bit, self-correcting Johnson (Token Ring) Counter (Fig. 25) [19]. A 74194 shift register was set up as a shift-left device. The output states and the desired switching sequence are provided in Table 6. Register QA (pin 15) was not used for the controller.

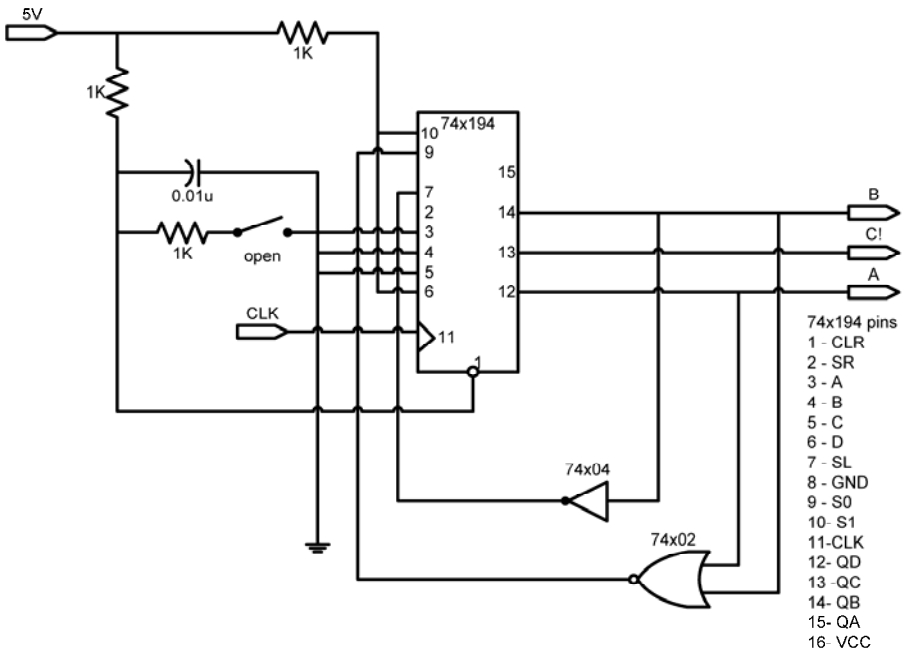

Figure 25. Self-Correcting Three State Johnson Counter [After Ref. 19]

STATE	QD	QC	QB	QA	INTERVAL	NOTES
	A	C!	B	n/a		Phases
A	1	0	0	X	0° – 60°	QA Register not used
B	1	1	0	X	60° – 120°	
C	1	1	1	X	120° – 180°	
D	0	1	1	X	180° – 240°	
E	0	0	1	X	240° – 300°	
F	0	0	0	X	300° – 360°	
Forbidden 1	0	1	0	X	n/a	Reset State
Forbidden 2	1	0	1	X	n/a	Next State Resets

Table 6. Self-Correcting Johnson Counter States

A 10 μs turn-on delay was implemented to allow the gate drivers to fully power up before the gate signals were propagated. This was accomplished with a simple RC filter to provide a temporary low signal to pin 1. The output of the QD register (pin 12) was labeled phase A, which determined the assignment of the other two phases. State A was selected as the initialization state for convenience. When the output of the QB register (pin 14) shifted, the complement was inserted into the QD register at the next clock. If a forbidden state is detected by the NOR gate, the machine then reloads the

initialization state (A) within two clock cycles. This counter only produces three states, each offset by 60 degrees. To create the six gate signals, an S-R latch was used where the S input is the complement of R (Fig. 26). This produces the output signals for all six switches of the PEBB. The signals produced by this circuit are presented in Table 7.

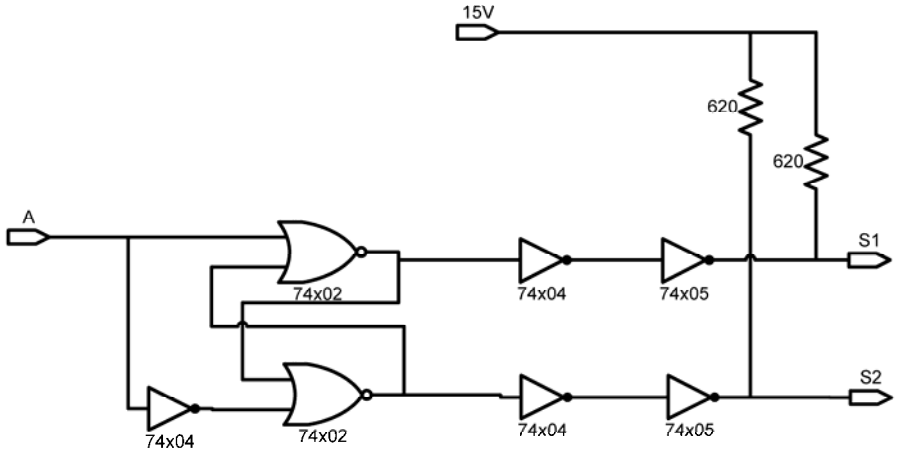

Figure 26. Gate Signal Generator Circuit (one phase only)

STATE	A	A!	C!	C	B	B!	INTERVAL
	Phase A		Phase C		Phase B		
	S1	S2	S6	S5	S3	S4	
A	1	0	0	1	0	1	0° – 60°
B	1	0	1	0	0	1	60° – 120°
C	1	0	1	0	1	0	120° – 180°
D	0	1	1	0	1	0	180° – 240°
E	0	1	0	1	1	0	240° – 300°
F	0	1	0	1	0	1	300° – 360°

Table 7. Six-State Machine Outputs

The outputs are now a representation of the six signals required for the six-state inverter and the switching sequence follows the desired pattern S1-S6-S3-S2-S5-S4 (see Fig. 11). The cascaded 7404/7405 inverters and the pull-up resistors were used to convert the 5V outputs produced by the counter to the 15V required by the gate drivers.

The relationship between the output frequency and the clock frequency is given by:

$$f_{clk} = 2nf_o, \tag{2.6}$$

where n is the number of bits in the counter, f_{clk} is the clock frequency and f_o is the output frequency for each signal. An output frequency of 60 Hz requires a clock frequency of 360 Hz.

A simple 555 timer circuit was constructed to produce the system clock (Fig. 27). The basis for this design was the astable circuit furnished in the datasheet [15].

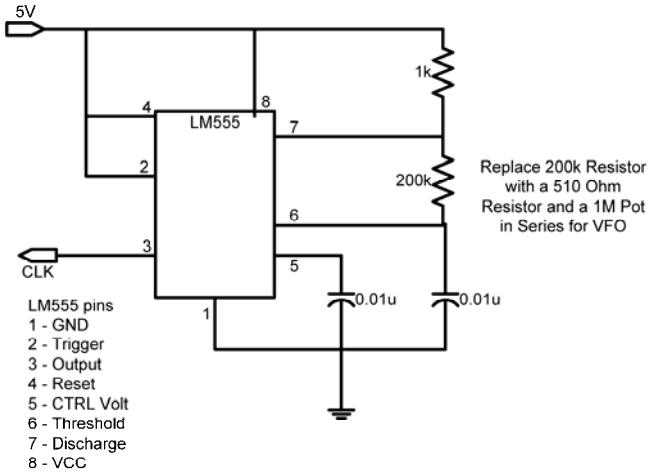

Figure 27. Bulk Controller Clock Circuit

To generate the clock frequency required by the counter the following relationship was used [15]:

$$f_{clk} = \frac{1.44}{(R_1 + 2R_2)C_1}, \tag{2.7}$$

where the resistor and capacitor values correspond to the positions indicated in Figure 26. The values for C_1 and R_1 were chosen to be $1\,\mu$F and $1\,k\Omega$ respectively. To achieve the required clock frequency of 360 Hz, R_2 needed to be $200\,k\Omega$.

By replacing the $200\,k\Omega$ resistor with a combination of $510\,\Omega$ in series with a $1\,M\Omega$ potentiometer, a variable frequency oscillator can be realized with a range of 7-7000 Hz. This will generate an associated system frequency of approximately 1-1000 Hz. For this thesis, the clock frequency is set at 360 Hz to produce a 60 Hz system.

C. HYSTERESIS CONTROLLER

The hysteresis controller was designed around the circuit built and tested in Reference 9 (Fig. 28). The logic of the associated S-R latch is provided in Table 8. Several modifications were necessary to make it compatible with the PEBB. A Hall-Effect Sensor (HES) circuit (with gain-balancing amplifiers) and a filter were coupled with the hysteresis circuit to create the entire controller (Fig. 29). The output of the comparators cannot ever produce the SR latch forbidden state as it is physically impossible for the output signal to be simultaneously above and below the tolerance band.

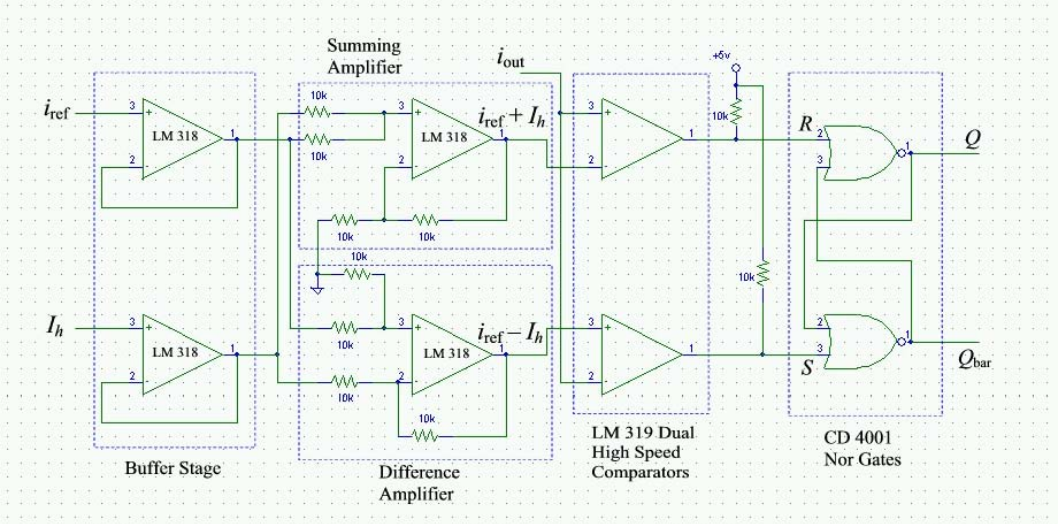

Figure 28. Hysteresis Controller Circuit (One Phase) [From Ref. 9]

LOGIC	S	R	Q	Q!	NOTES
i_o in the band	0	0	Last Q	Last Q!	No gate signal change.
$i_o \geq i_{ref} + \Delta_h$	0	1	0	1	S2 gate signal (Phase A)
$i_o \leq i_{ref} - \Delta_h$	1	0	1	0	S1 gate signal (Phase A)
Impossible	1	1	X	X	Forbidden State for SR latch

Table 8. S-R Latch Logic

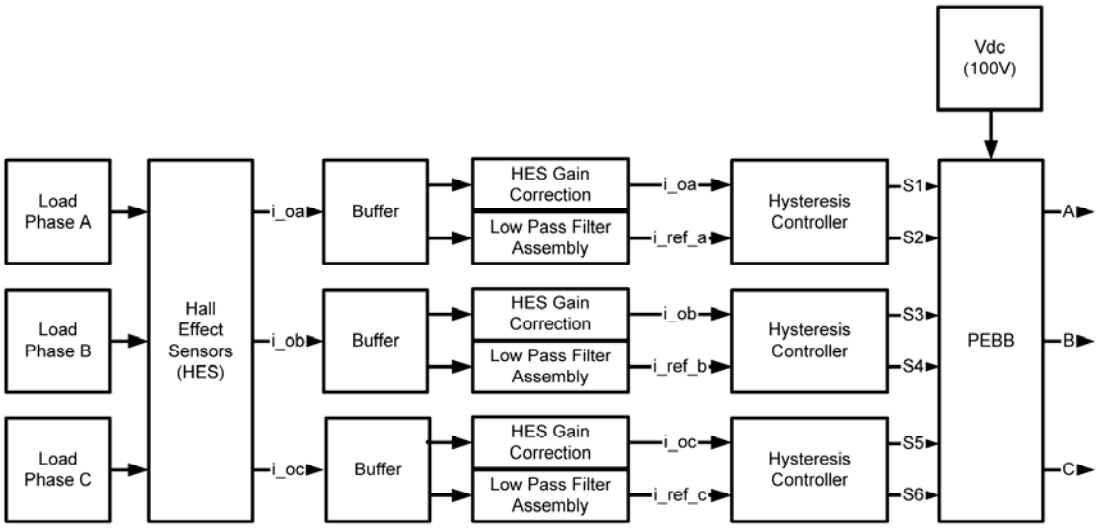

Figure 29. Hysteresis Controller Block Diagram

1. Hysteresis Controller Redesign

Several modifications were required to allow the controller to drive the PEBB (Fig. 30). The pull up voltage was increased to 15V and the pull up resistors to $30\ k\Omega$ in order to provide the correct gate control signal voltage. A second S-R latch coupled with a 100 kHz RC filter was added to enable the first latch to allow the PEBB gate drivers to power-up completely before receiving gate control signals. The delay produced was $1\ ms$ (100 times greater than the bulk controller delay), which allowed the bulk inverter to produce a waveform. This, in turn, ensured that a valid reference was received by the hysteresis controller at start-up. The necessary start-up delay for the PEBB gate drivers was also guaranteed with this set-up. The logic for the enable circuit is shown in Table 9. Finally, the four LM318 op-amps used in Reference 9 were replaced with one LM324 quad op-amp. This was done for convenience and had minimal effect on the circuit performance.

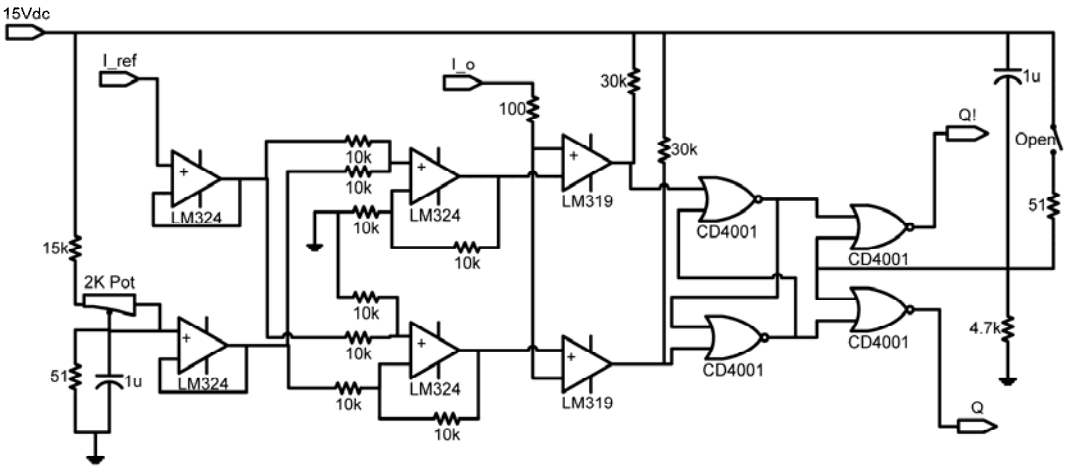

Figure 30. Modified Hysteresis Circuit (one phase only)

S	R	EN	Q	Q!	NOTES
0	0	0	Last Q	Last Q!	No gate signal change
0	1	0	0	1	S2 gate signal (Phase A)
1	0	0	1	0	S1 gate signal (Phase A)
0	0	1	0	0	$10\mu s$ Power-up Delay/Reset
0	1	1	0	0	
1	0	1	0	0	

Table 9. S-R Latch with Enable

2. Hall-Effect Sensor (HES) Module

The current detection circuit designed to obtain the output current feedback signal and the reference sine wave for the hysteresis circuit was built using three FW Bell CLN-50 HES (Fig. 31). The circuit is identical to the one recommended in the datasheet. A dual-output dc-dc converter was used to convert $24\,V_{dc}$ to $\pm 15\ V_{dc}$ to power the circuit.

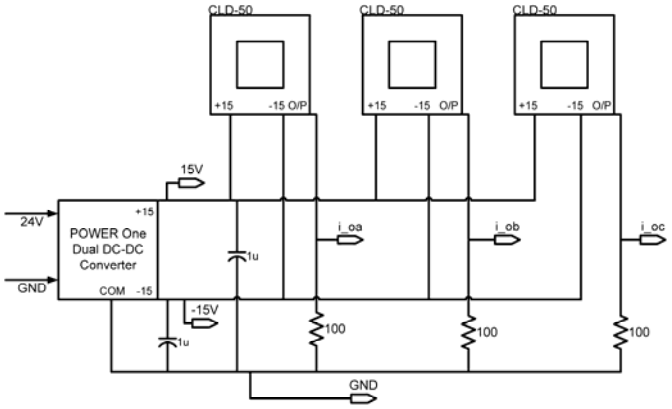

Figure 31. Hall Effect Sensor Circuit

3. Filter Assembly

A low-pass filter assembly was needed to extract the fundamental frequency from the higher order harmonics in the load current obtained by the Hall-effect sensors. The topology used is shown below (Fig. 32). The outputs from the HES were balanced using an amplifier and the conditioned output was sent to the hysteresis controller and the low-pass filter. The LM324 op-amps had a 10 μs delay which is negligible for a 60 Hz system frequency. The low-pass filter smoothed out the current waveform to create the hysteresis reference and a cascaded all-pass filter and amplifier circuit were used to correct the post filtering gain and phase shifts.

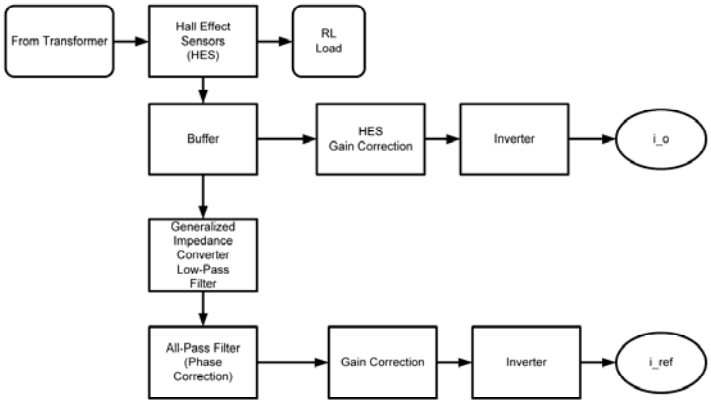

Figure 32. Filter Block Diagram

The HES amplifier circuit was designed using two simple inverting op-amp circuits to manually equalize the outputs of the three phases (Fig. 33). A switch allowed this stage to be excluded from the system for test purposes.

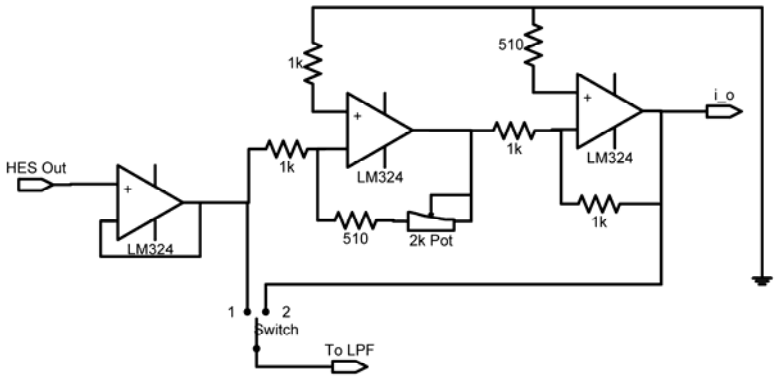

Figure 33. HES Equalization and Amplification Stage

The filter design uses the generalized impedance converter (GIC) bi-quad filter (Fig. 34). The GIC is a universal filter that can be modified to produce any filter type by inserting resistors and/or capacitors into the circuit where required (Table 10). The advantage of using a GIC is that it has a simple design, has low sensitivity to impedance value variations and has a maximally flat response. The main disadvantage is that the filter can only be optimized for a limited frequency range, and is unsuitable for variable frequency operation.

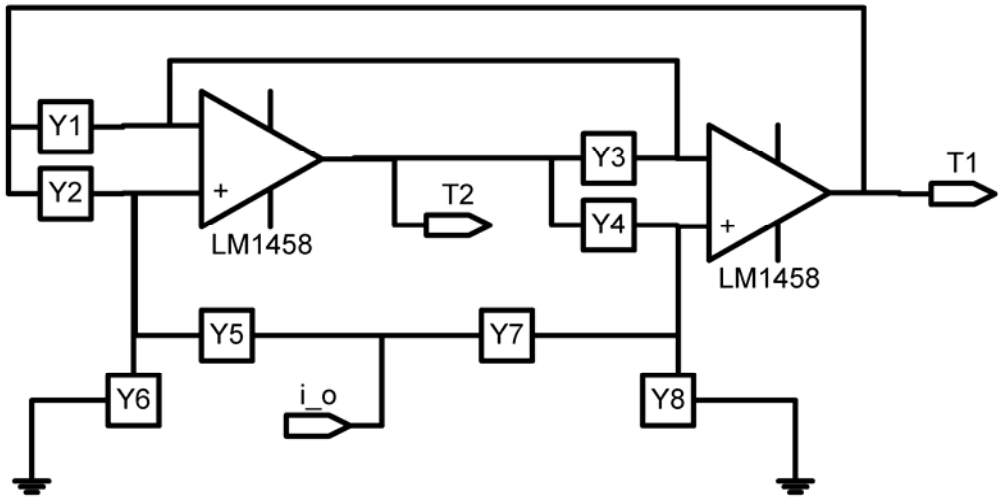

Figure 34. The Generalized Impedance Converter (GIC) [From Ref. 18]

FILTER	Y1	Y2	Y3	Y4	Y5	Y6	Y7	Y8	OUTPUT NODE
LP	G	Y	Y+B	G	G	0	0	G	T2
HP	G	G	Y	G	0	G	Y	B	T1
BP	G	G	Y	G	0	G	B	Y	T1
Notch	G	G	Y	G	G	0	Y	B	T2
AP	G	G	Y	G	G	0	Y	B	T1
	$Y = sC;\ G = \frac{1}{R};\ B = \frac{G}{Q_p}$								

Table 10. GIC Filter Design Implementation

The transfer functions for this filter are [18]:

$$T_1 = \frac{Y_1Y_4Y_5 + Y_3Y_7(Y_2+Y_6) - Y_3Y_5Y_8}{Y_1Y_4(Y_5+Y_6) + Y_2Y_3(Y_7+Y_8)}; \tag{2.8}$$

and

$$T_2 = \frac{Y_1Y_4Y_5 + Y_1Y_5Y_8 + Y_2Y_3Y_7 - Y_1Y_6Y_7}{Y_1Y_4(Y_5+Y_6) + Y_2Y_3(Y_7+Y_8)}. \tag{2.9}$$

Because the system frequency was so low, the op-amps were assumed to be ideal in all calculations. An analysis of the system using the non-ideal op-amp equations would be necessary for system frequencies higher than 2 kHz. A derivation of the non-ideal transfer functions for the GIC is provided in Appendix B.

To design a second-order Butterworth Low-pass Filter (LPF), the quality factor, Q_p, was set to $\frac{1}{\sqrt{2}}$. A capacitance of 1 μF was chosen to scale the resistors appropriately. The resistor values were found by using the relationship [18]:

$$\omega_{co} = 2\pi f_{co} = \sqrt{\left(\frac{Q_p - 1}{Q_p}\right)\left(\frac{1}{RC}\right)^2}. \tag{2.10}$$

Since the output current is expected to contain fifth harmonic and higher component values, a cutoff frequency of slightly less than the fifth harmonic, 250 Hz, was chosen. Solving the equation, the resistance required is $989\ \Omega$. The closest standard resistor value of $1\ k\Omega$ was selected to provide a close approximation of the desired value and to simplify the design calculations. The configuration of the LPF is shown below (Fig. 35). The resistor values chosen for R5 and R1 produce a quality factor of 0.707R which ensures a Butterworth response. As Table 10 indicates, Equation 3.4 is the transfer function used for the GIC based LPF configuration.

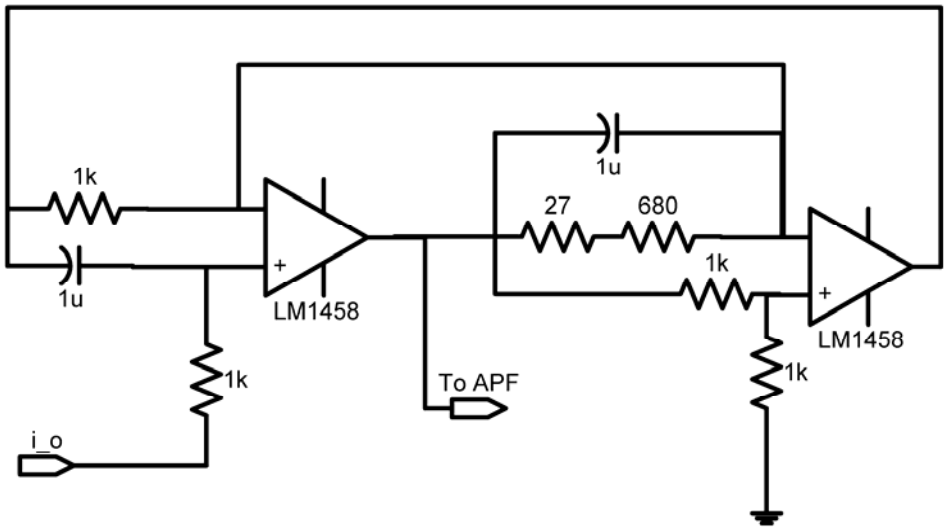

Figure 35. The Low-pass Filter Circuit

The frequency response of this filter was simulated in MATLAB using the transfer function for the LPF:

$$T^2 = \frac{2}{\left(1*10^{-6}\right)s^2 + \left(1.414*10^{-3}\right)s + 1} \tag{2.11}$$

The frequency response of this system is shown in Figure 36. The blue lines represent the ideal op-amp performance; the green lines represent the non-ideal case. The system frequency responses are nearly identical for frequencies below 2 kHz. Frequencies greater than 2 kHz require that a non-ideal op-amp analysis be used to perform frequency response analysis. The MATLAB code used to perform the filter analysis is given in Appendix A and the derivation of the non-ideal case is presented in Appendix B. The calculated phase shift is -31.9 degrees and the gain is 5.92 dB at a system frequency of 60 Hz. The filter roll-off frequency is 180 Hz and the maximum operational frequency for this filter is 195 Hz.

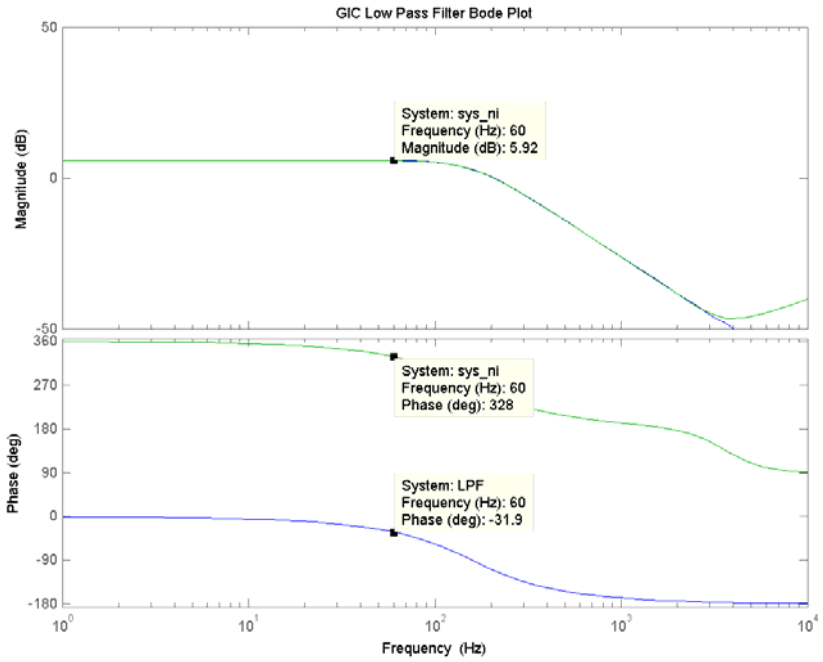

Figure 36. Low-pass Filter Bode Plot

To phase-correct and gain-correct the output of the LPF, an all-pass filter (APF) and an amplifier were cascaded in series. The design for the APF was identical to the one used in Reference 10 (Fig. 37) [19].

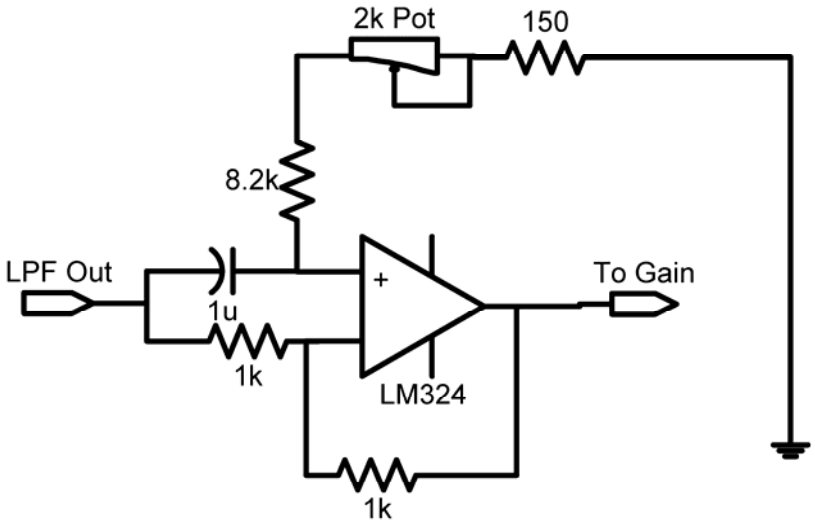

Figure 37. All-Pass Filter Design (Lead Configuration)

To correct the LPF output, the APF output needs to lead the input by 31.9 degrees. The equation used to determine the resistor and capacitor values required to implement this shift is [19] (calculation provided in Appendix B):

$$\theta(\omega) = 32^{\circ} = 180^{\circ} - 2\tan^{-1}(\omega RC). \tag{2.12}$$

A 1 μF capacitor was chosen for this filter. For a system radian frequency 377 $\frac{\text{rad}}{\text{s}}$, a 9.281 k$\Omega$ resistor is needed between pin three of the op-amp and ground. A voltage divider using a 2 kΩ potentiometer in series with an 8.3 kOhm resistor and a 150 Ohm resistor was used in the circuit to provide exact phase matching with the LPF. This APF design is more frequency limiting than the LPF and sets the optimum system frequency. The optimum operational frequency of the system is set at 60 Hz with this design. The transfer function for the APF is:

$$T_{APF} = \frac{sRC - 1}{sRC + 1},$$

or

$$T_{APF} = \frac{s\left(9.281*10^{-3}\right) - 1}{s\left(9.281*10^{-3}\right) + 1} \tag{2.13}$$

To correct the effects of the LPF gain, a circuit was designed using two inverting op-amps (Fig. 38).

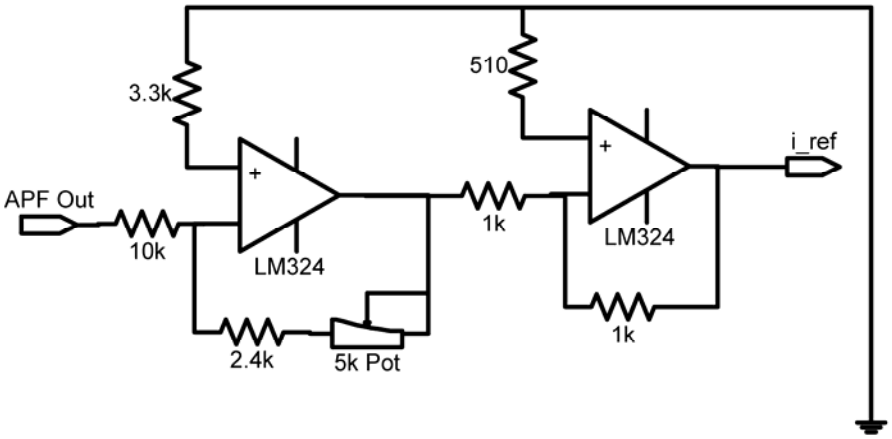

Figure 38. Gain Correction Circuit

The first stage provides a gain correction range of 0.24 to 0.74 (nominal value 0.50582). This allows the output to be precisely corrected. Since the amplifier inverts the input, a second inverting stage with unity gain is used to phase correct the output.

To evaluate the frequency response of the entire filter system, the transfer functions of the LPF, APF, and Gain Correction stages were multiplied together.

$$T_{SYS} = G*T_2*T_{APF} \tag{2.14}$$

where G is the nominal gain of the gain-correction circuit (G = 0.50582). The total system transfer function:

$$T_{SYS} = \frac{\left(9.281*10^{-3}\right)s - 1}{\left(9.281*10^{-9}\right)s^3 + \left(1.408*10^{-5}\right)s^2 + \left(1.066*10^{-2}\right)s + 1} \tag{2.15}$$

The frequency response of this system shows that the gain is near unity and the phase shift is near zero at 60 Hz (Fig. 39).

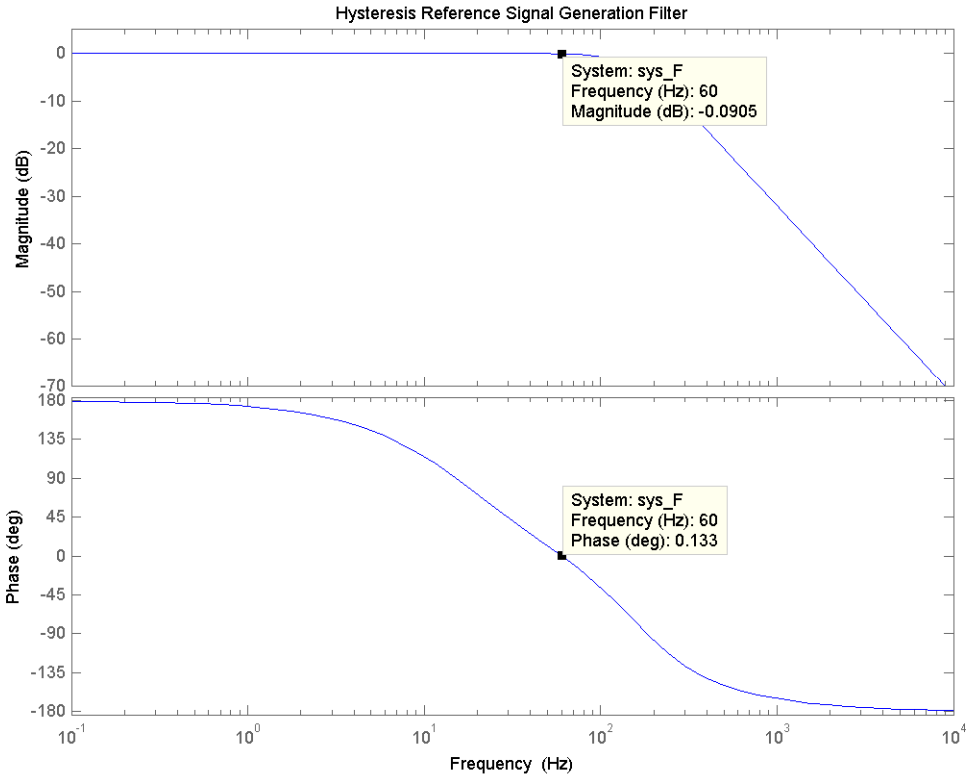

Figure 39. Filter System Bode Plot

D. SUMMARY

This chapter provided the designs used to implement the bulk six-step and the hysteresis controllers. Specific designs covered were: the bulk six-step controller, the Hall Effect sensor circuit, the filter circuit, and the modified hysteresis circuit. The controller design for this thesis produces a 60 Hz output of the bulk controller and generates a manually adjustable phase and gain correction to tune the reference waveform for the hysteresis controller.

The ideal bulk controller would allow variable system frequencies. The ideal hysteresis controller would sense the system frequency and automatically adjust the gain and phase correction of the reference waveform to match the load current. The use of a Field Programmable Gate Array (FPGA) or a Programmable Logic Device (PLD) would simplify the construction of the controllers and provide the frequency independence required by a variable frequency bulk inverter.

IV. COMPUTER MODEL AND SIMULATION

A. OVERVIEW

This chapter describes the model created to simulate the PCHI system in SIMULINK. The results will baseline the expected system performance. Specific topics of discussion include: a simulation system overview, the three-phase half-bridge inverter model, the system load model, the bulk six-step controller model and the hysteresis controller model.

Certain assumptions are made to simplify the model. First, the system's three-phase load is linear and balanced. Further, the model is temperature independent, which is to say there will be no time-variance in the output due to system heating or cooling. The IGBTs as modeled are assumed to act as ideal switches with no switching delays, no current leakages, or no voltage drops. No resistive losses other than those associated with the load were considered in this model. The start-up delays for both controllers were also not implemented in the model. Even with these assumptions, the model is quite accurate, due to the small effect the errors have on the simulation results.

Figure 40 illustrates the PCHI SIMULINK model. The calculations used in it will be presented for the three-phase half-bridge inverter, the six-step controlled inverter and the hysteresis controlled inverter. It consists of the following major component modules: a bulk six-step controller, a hysteresis controller, two Semikron PEBBs (a six-step controlled and a hysteresis controlled), the system load, and a dq0-reference frame analysis module. Each component will be described in detail in the next sections.

The system inputs were called when the model was run. Specific system inputs provided were the simulation run time, the dc bus voltage (rail-to-rail), the system frequency, the bandwidth, the load inductances and resistances, and the six-step controller pulse phase delays. The values used to model the lab system are provided in Table 11. After the simulation, the various performance parameters saved in the MATLAB workspace were plotted versus time to analyze the system performance. All m-files and SIMULINK schematics for the model are contained in Appendix A.

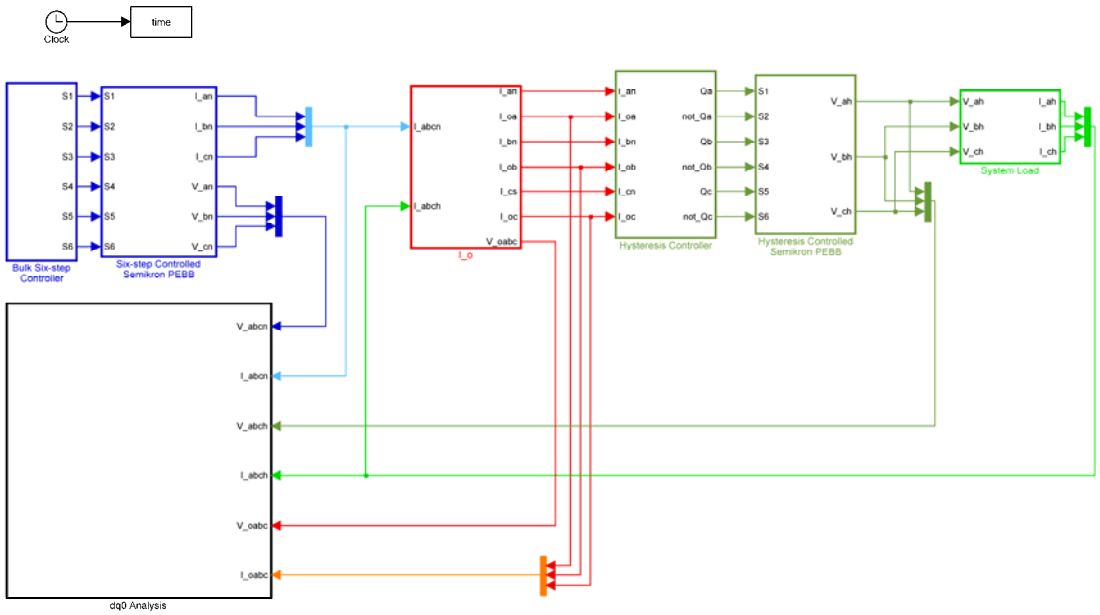

Figure 40. SIMULINK Model of the Parallel-Connected Hybrid Inverter System

CONSTANT	VALUE
Start Time (t_start)	0 seconds
Stop Time (t_stop)	0.25 seconds
DC Bus Voltage (Vdc)	100 Volts
System Frequency (f_c)	60 Hertz
B Pulse Phase Delay (B)	$\frac{2}{6f_c}$
C Pulse Phase Delay (C)	$\frac{4}{6f_c}$
Delta h (hysteresis tolerance half bandwidth) (delta_h)	0.05
Coupling Inductor Inductance (L_c)	2.5 mH
Coupling Inductor Resistance (worst case value expected) (R_c)	25 mΩ
Load Inductance (L_l)	20 mH
Load Resistance (R-l)	10 Ω
Harmonics Calculation Index (n)	21

Table 11. SIMULINK Model Input Values

B. SEMIKRON IGBT BASED PEBB MODELS

Both PEBB modules are identical in operation. The model utilizes six binary position switches to simulate the three IGBT half-bridges (Fig. 41). The six switch positions are driven by the gate control signals provided by the two different controllers. At no time are both the upper and lower switches on at the same time.

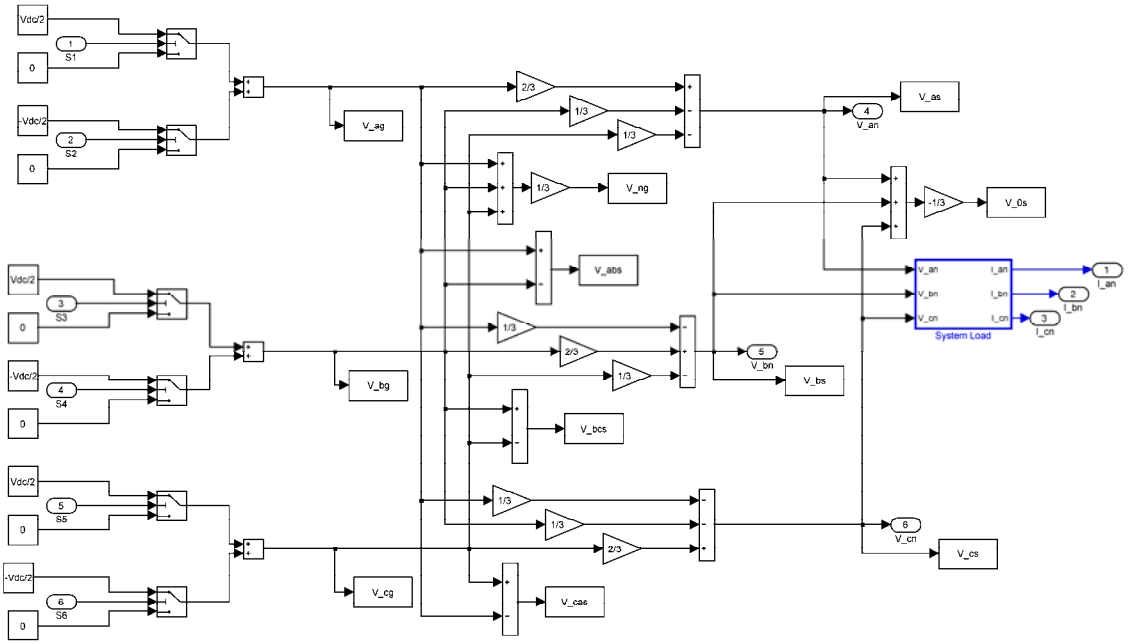

Figure 41. Bulk Six-step Controlled PEBB Module

The single-phase line-to-ground voltages of the three legs are shown as v_{ag}, v_{bg}, and v_{cg}, and the line-to-neutral voltages of the three phases are designated v_{an}, v_{bn}, and v_{cn}. The line-to-ground voltages are referenced from the midpoint of the IGBT half-bridge for each phase to the mid-potential point between the capacitors. The line-to-neutral voltages are referenced from the mid-point of the IGBT half-bridge to the center of the wye-connected load. Once all of the line-to-ground voltages are found, the line-to-line voltages can be calculated by [12]:

$$\begin{aligned} v_{ab} &= v_{ag} - v_{bg} \\ v_{bc} &= v_{bg} - v_{cg} \\ v_{ca} &= v_{cg} - v_{ag} \end{aligned} \quad . \qquad (4.1)$$

Because the system is wye-connected then the relationship between the line-to-neutral and the line-to-ground voltages is [12]:

$$\begin{aligned} v_{ag} &= v_{an} + v_{ng} \\ v_{bg} &= v_{bn} + v_{ng} \\ v_{cg} &= v_{cn} + v_{ng} \end{aligned} \tag{4.2}$$

where

$$v_{ng} = \frac{1}{3}\left(v_{ag} + v_{bg} + v_{cg}\right) - \frac{1}{3}\left(v_{an} + v_{bn} + v_{cn}\right). \tag{4.3}$$

The term v_{0s} is the zero-sequence voltage which is identically equal to zero for ideally balanced loads. It can be calculated by [12]:

$$\frac{1}{3}\left(v_{an} + v_{bn} + v_{cn}\right) = v_{0s}. \tag{4.4}$$

By removing the zero sequence term from equation (4.3) and solving for the line-to-neutral voltages the following results are obtained [12]:

$$\begin{aligned} v_{an} &= \left[\frac{2}{3}v_{ag} - \frac{1}{3}v_{bg} - \frac{1}{3}v_{cg}\right] \\ v_{bn} &= \left[\frac{2}{3}v_{bg} - \frac{1}{3}v_{ag} - \frac{1}{3}v_{cg}\right] \\ v_{cn} &= \left[\frac{2}{3}v_{cg} - \frac{1}{3}v_{ag} - \frac{1}{3}v_{bg}\right]. \end{aligned} \tag{4.5}$$

These calculations form the basis of the PEBB model voltage outputs. All of the inductors in the model are interconnected, but only the currents through the coupling inductors are used to produce the state variables for the circuit analysis. In the model all of the coupling inductors are identical and are modeled as a series LR load. All output values were sent to the workspace as arrays. A time reference vector was generated to ensure that all output vector lengths were identical for plotting purposes.

The following Kirchhoff's Voltage Law (KVL) equations are used for the network [21]:

$$-V_{agh} + L_c \frac{d}{dt} i_{anh} + R_c i_{anh} + L_l \frac{d}{dt}\left(i_{anh} + i_{anb}\right) + R_l\left(i_{anh} + i_{anb}\right) + V_{ng} = 0 \qquad (4.6)$$

$$-V_{bgh} + L_c \frac{d}{dt} i_{bnh} + R_c i_{bnh} + L_l \frac{d}{dt}\left(i_{bnh} + i_{bnb}\right) + R_l\left(i_{bnh} + i_{bnb}\right) + V_{ng} = 0 \qquad (4.7)$$

$$-V_{cgh} + L_c \frac{d}{dt} i_{cnh} + R_c i_{cnh} + L_l \frac{d}{dt}\left(i_{cnh} + i_{cnb}\right) + R_l\left(i_{cnh} + i_{cnb}\right) + V_{ng} = 0 \qquad (4.8)$$

$$-V_{agh} + L_c \frac{d}{dt} i_{anh} \; R_c i_{anh} - L_c \frac{d}{dt} i_{anb} - R_c i_{anb} + V_{agb} = 0 \qquad (4.9)$$

$$-V_{bgh} + L_c \frac{d}{dt} i_{bnh} \; R_c i_{bnh} - L_c \frac{d}{dt} i_{bnb} - R_c i_{bnb} + V_{bgb} = 0 \qquad (4.10)$$

$$-V_{cgh} + L_c \frac{d}{dt} i_{cnh} \; R_c i_{cnh} - L_c \frac{d}{dt} i_{cnb} - R_c i_{cnb} + V_{cgb} = 0 \qquad (4.11)$$

$$i_{ox} = i_{xnh} + i_{xnb}, \; x = a, b, \text{ or } c. \qquad (4.12)$$

All of the equations were split into component parts, bulk inverter and hysteresis inverter, to calculate the current of each inverter separately. The load current could then be determined by superposition. Ohm's law is applied to each phase voltage using the impedance of the entire phase leg (Fig. 42) to produce the current waveforms from the PEBB voltages.

$$I_b = \frac{V_b}{Z} \qquad (4.13)$$

where:

$$Z = \left(L_c + L_l\right)s + \left(R_c + R_l\right). \qquad (4.14)$$

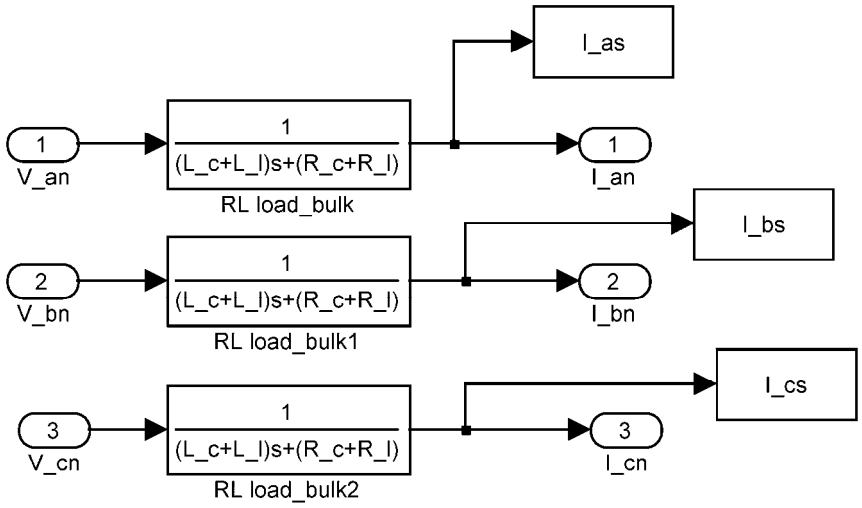

Figure 42. Load Module (Bulk Inverter Shown)

C. BULK CONTROLLER MODEL

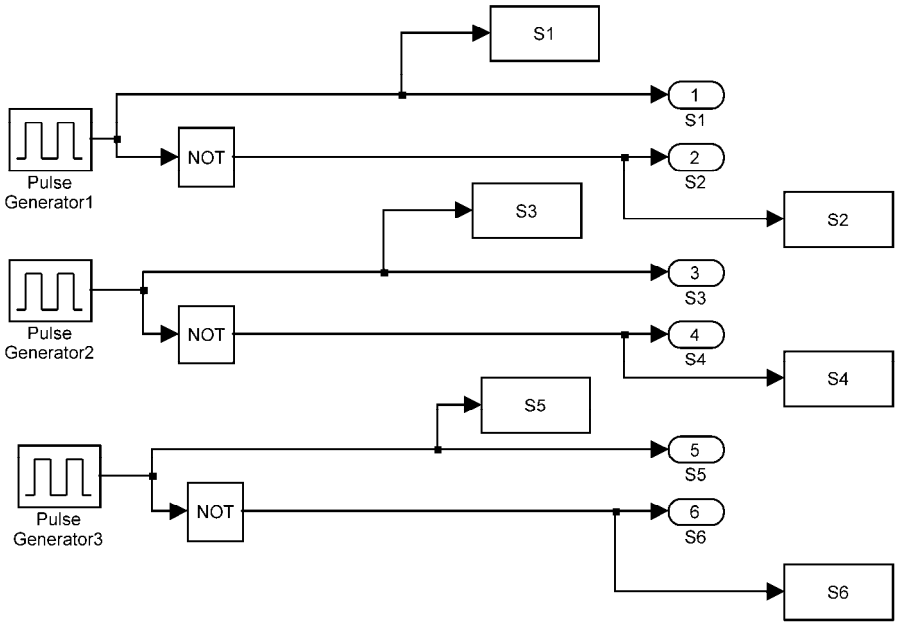

Figure 43. Bulk Six-Step Controller Model

The bulk six-step controller (Fig. 43) was created using three pulse generators to produce the six gate control signals. The pulse generator parameters used were: unity

amplitude, pulse width of 50 (50% duty cycle), and time based. The period of the system (16.67 ms) was input to the model at start-up. Phase B was given a delay of one-third of a period and Phase C was delayed two-thirds of a period for standard three-phase operations. Each pulse generator provided a phase signal and its complement to create the six gate signals. The signals (S1-S6) matched the expected results as defined in Table 3 (Fig. 44).

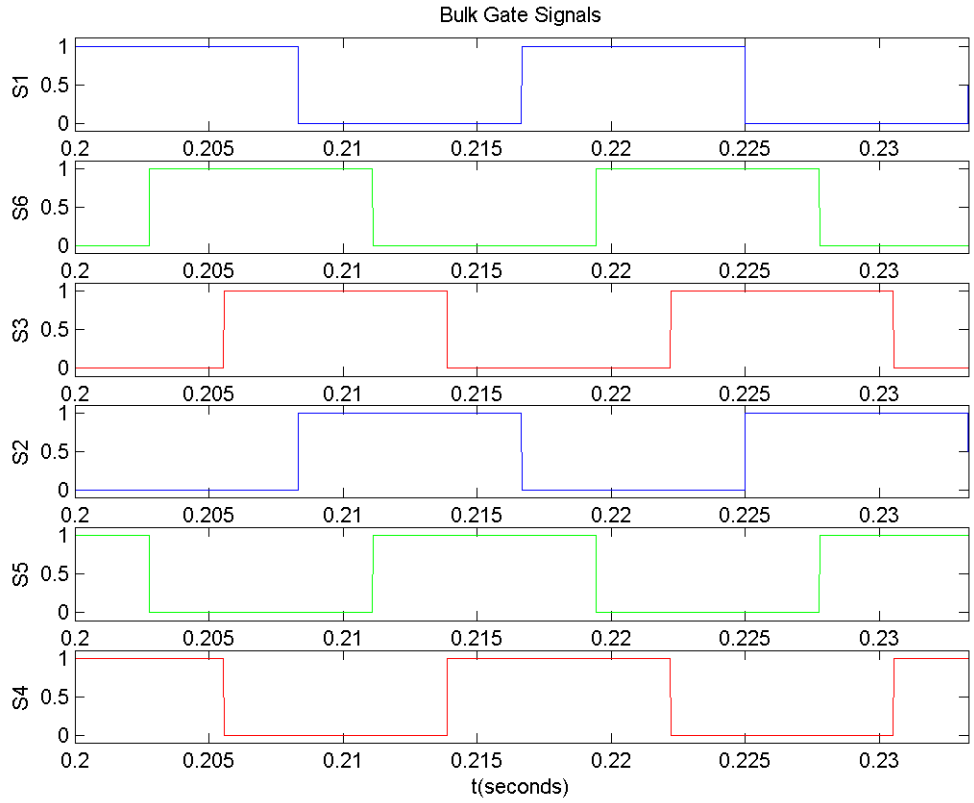

Figure 44. Bulk Six-Step Gate Control Signals

The resultant line-to-line voltages, line-to-neutral voltages and the current waveforms generated by the bulk six-step controlled PEBB also match the expected values tabulated in Table 4 (Figs. 45-47).

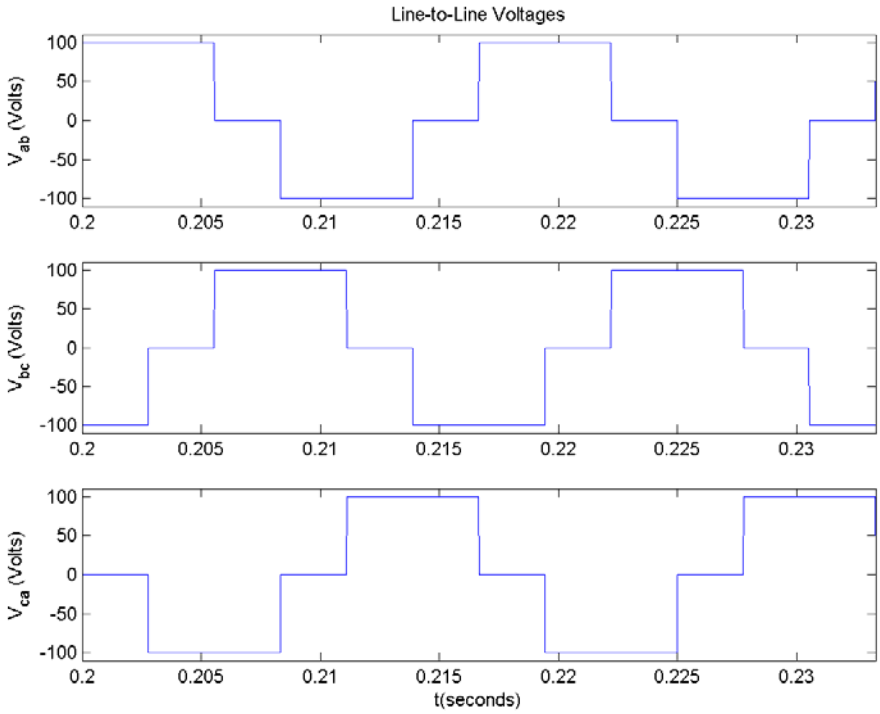

Figure 45. Bulk Inverter Line-to-Line Voltages

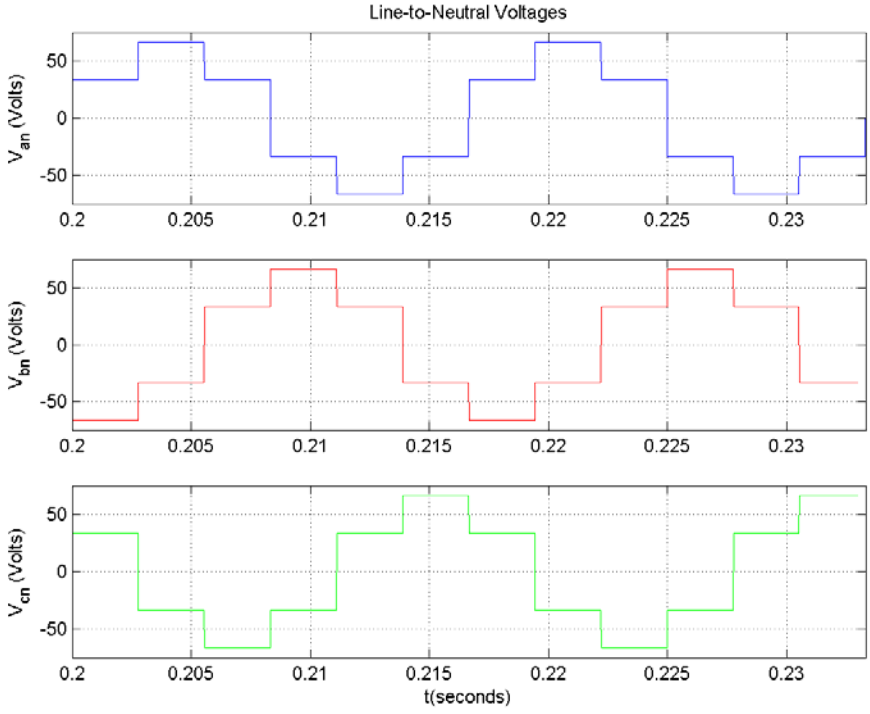

Figure 46. Bulk Inverter Line-to-Neutral Voltages

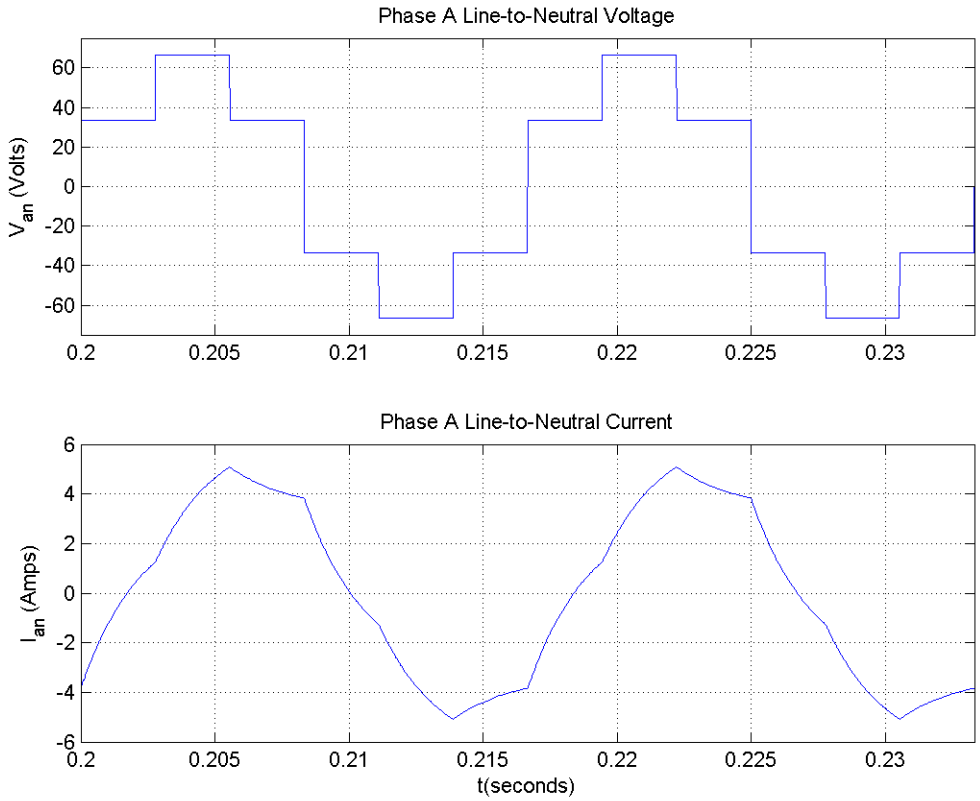

Figure 47. Bulk Inverter Voltage (top) and Current (bottom) Waveforms

All wave shapes obtained agree with published data for similar six-step controlled inverter systems [11]. The bulk model therefore provides a reliable simulation for the bulk inverter system.

D. HYSTERESIS CONTROLLER MODEL

To simulate the hysteresis controller the load current for each phase was passed through an LPF, a gain correction, and an APF. The transfer functions used are those calculated in Chapter III while the gain used was the nominal value of 0.50582. The resultant reference waveform then had the selected tolerance band offset (0.05%) added and subtracted to it to produce the hysteresis band. The load current was then compared to the tolerance band to produce the gate control signals (Fig. 48).

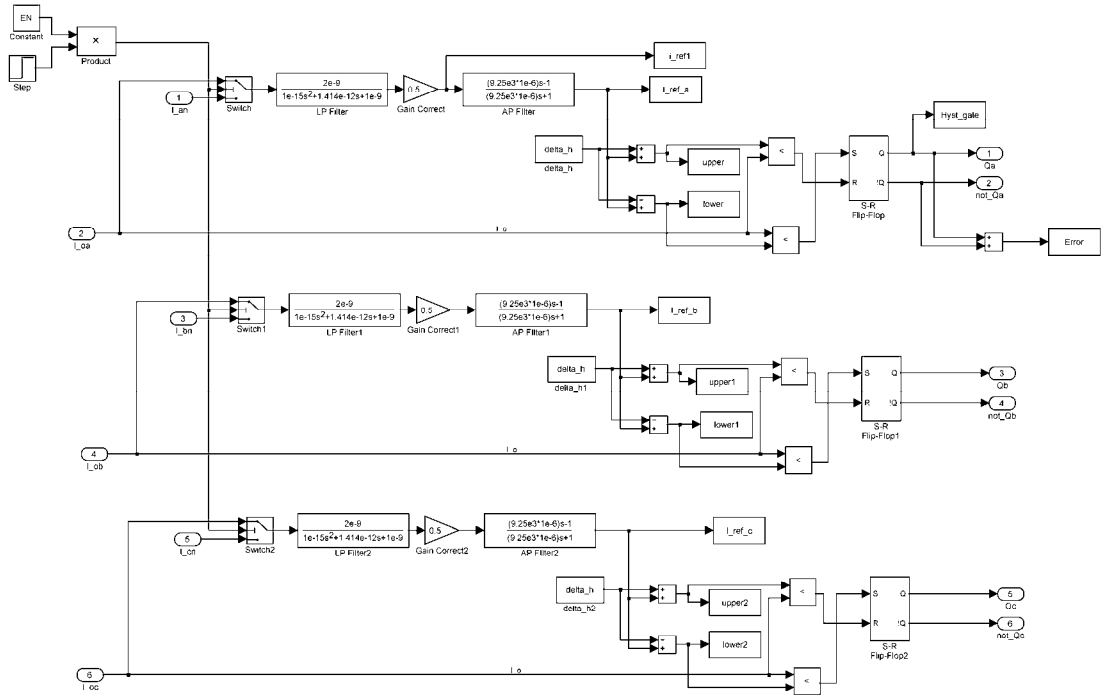

Figure 48. Hysteresis Controller SIMULINK Model

The hysteresis controller generated the gate control signals described in Table 5 (Fig 49). The blue plots are for phase A (S1 and S2), the red plots for phase B (S3 and S4) and the green plots are for phase C (S5 and S6). Note that the gate control signals of the phase leg switches are complimentary (S2 is the complement of S1, S4 of S3 and S6 of S5). The switching frequency of the hysteresis controller is noticeably variable.

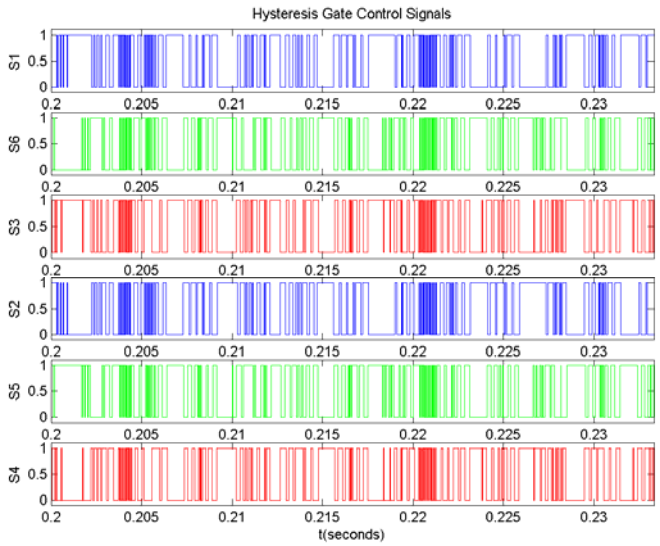

Figure 49. Hysteresis Controller Gate Control Signals

In the three-phase system there is virtually no correlation between the reference waveform amplitude and the switching frequency observed (Fig. 50). Since the hysteresis inverter is not constructed of three isolated H-bridges, but rather of three inter-dependant half-bridges, a switching transition in one phase affects the current amplitude in the other two phases. This is called cross-phase interference. The random nature of the cross-phase interference makes modeling extrapolations from a single-phase system to a three-phase system next to impossible as was discovered in this thesis.

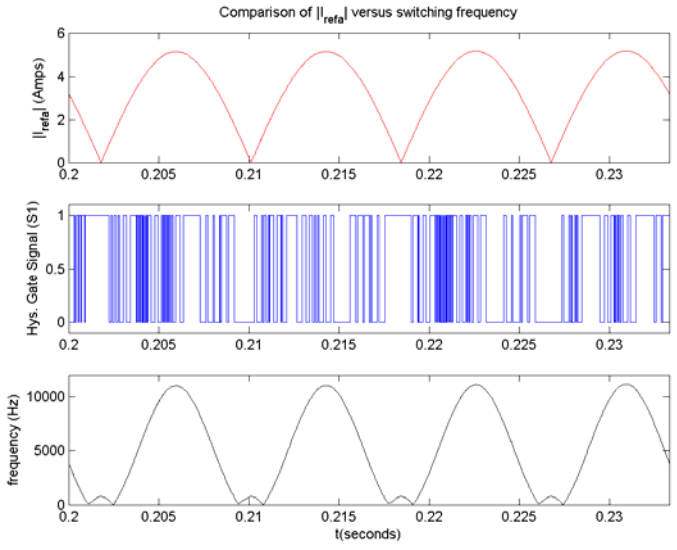

Figure 50. Switching Frequency Performance

It is, however, possible to estimate the limits of the switching frequency based on the single phase model. The maximum calculated switching frequency using the single-phase switching frequency equation (Equation 2.5) is 11.1 kHz and the minimum frequency is 495 Hz. The maximum frequency expected for this system with the 10% margin of error added is 13 kHz, which is well within the frequency limits of the PEBB.

The reference waveform obtained is a nearly ideal sinusoid (Fig. 51). The bulk current is shown in blue (distorted waveform), the gain corrected output of the LPF is shown in red (delayed sinusoid), and the APF output, the reference, is shown in green (phase corrected sinusoid). The hysteresis controller model provided the option of using the improved load current to generate a "double-filtered" reference signal. The reference waveform produced by the filtered hybrid load current shows marked improvement over initial filtered bulk current reference signal (Fig. 52). This models more precisely what is expected in the laboratory build prototype controller.

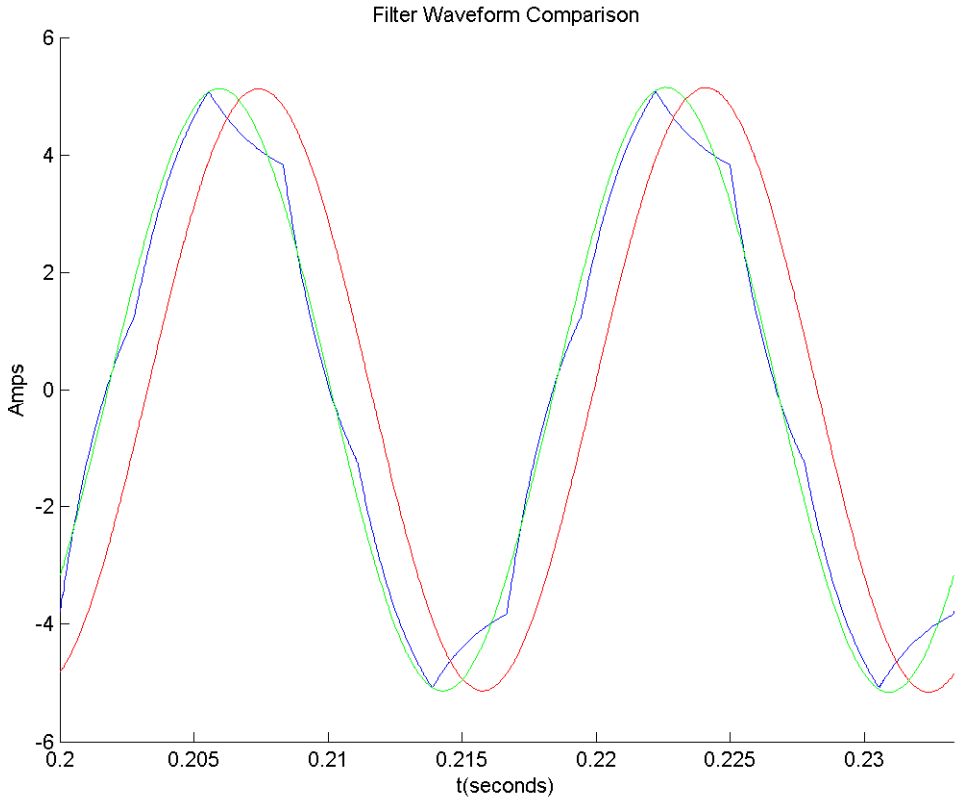

Figure 51. Hysteresis Controller Filter Performance

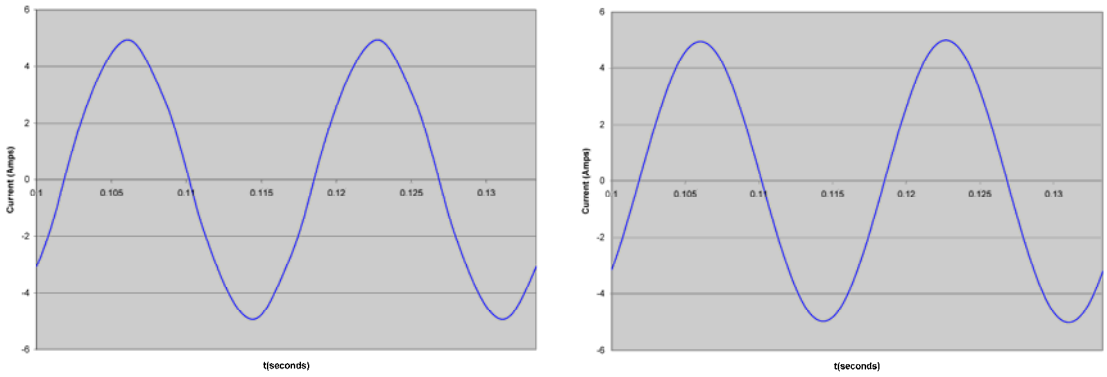

Figure 52. Reference Waveform Improvement due to Double Filtering. Left: Initial reference signal. Right: Final (improved) reference signal

A representation of the three reference signals shows the three-phase reference system with the waveforms offset 120° from each other (Fig. 53). The references for the hysteresis controller thus form the three-phase structure for creating the tolerance bands.

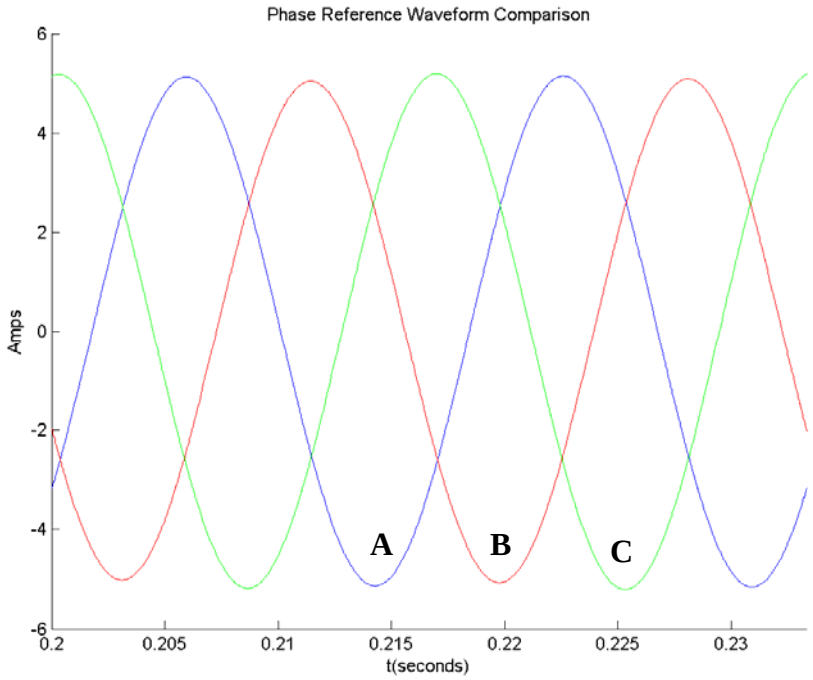

Figure 53. Three-phase Reference Waveforms: phase A (blue), phase B (red), phase C (green)

Figure 54 shows the output current waveforms for the three phases. The current stays within the tolerance bands as expected. The cross-phase interference effects are noticeable in the output. This further demonstrates that each phase is codependent on the other two. Distortion appears to be higher at the maxima and minima of the waveforms.

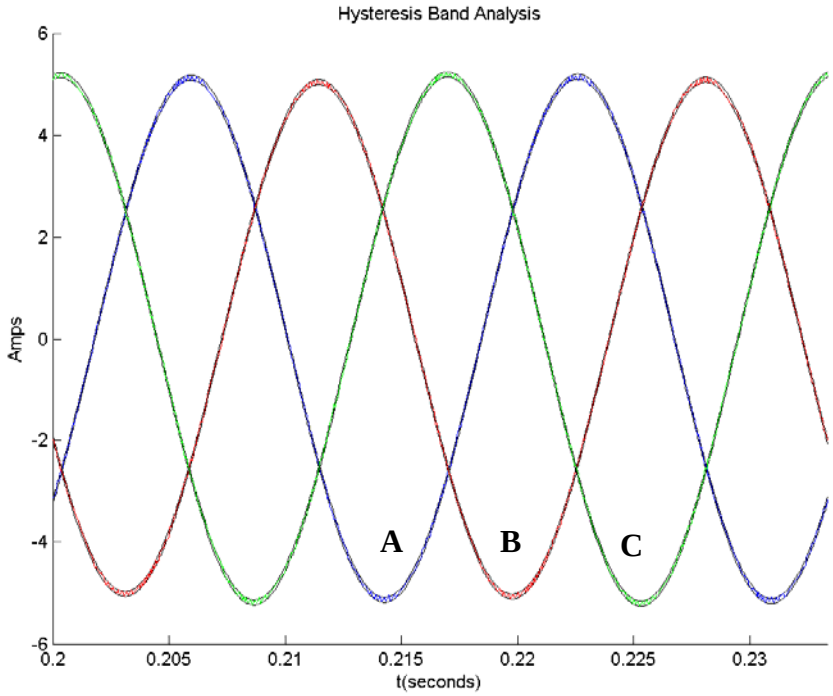

Figure 54. Three-phase Hysteresis Band Performance. Phase A (blue), Phase B (red) and Phase C (green)

The hysteresis inverter current generated by the feedback loop is of particular interest (Fig. 55). If the reference waveform gain correction and the phase correction are properly adjusted, there will be no fundamental frequency component in the generated waveform, only higher harmonics. The current waveform produced by the model demonstrates that there is little noticeable fundamental frequency in the current generated. The pattern repeats itself every 16.67 ms as expected. The amplitude of the hysteresis current should only be enough to cancel the harmonic content of the bulk inverter. This will be tested by superimposing the hysteresis current onto the bulk inverter current in the hybrid system model.

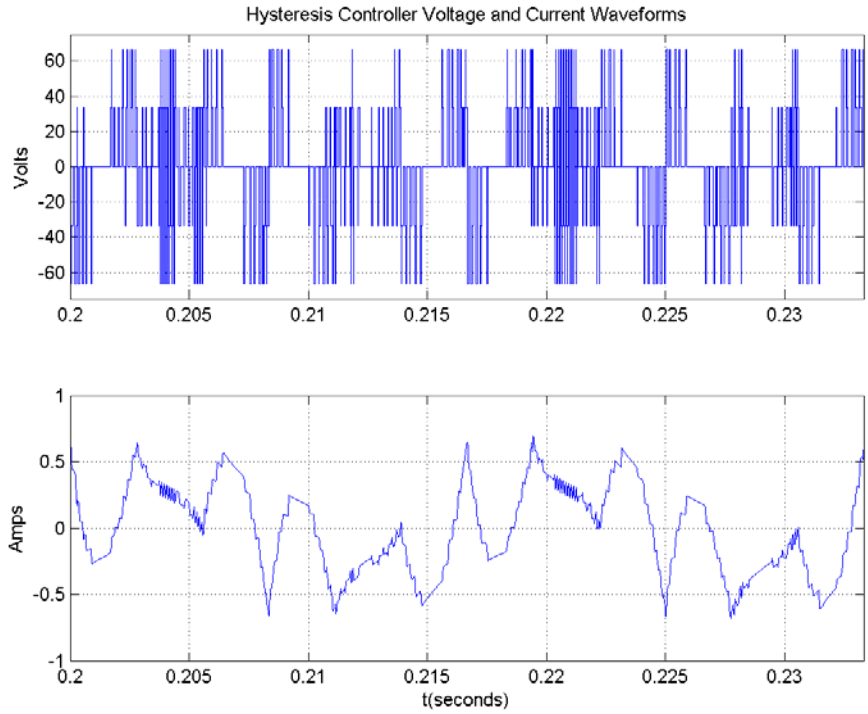

Figure 55. Hysteresis Inverter Voltage (top) and Current (bottom) Waveforms

E. THE SYSTEM OUTPUT

Figure 56 provides a comparison of the bulk inverter outputs and the hysteresis inverter outputs. The goal of the PCHI scheme is to ensure that the superposition of the bulk and hysteresis inverter currents produce a nearly perfect sinusoidal output. The hysteresis inverter will therefore act as an active low-pass filter, effectively canceling the harmonics.

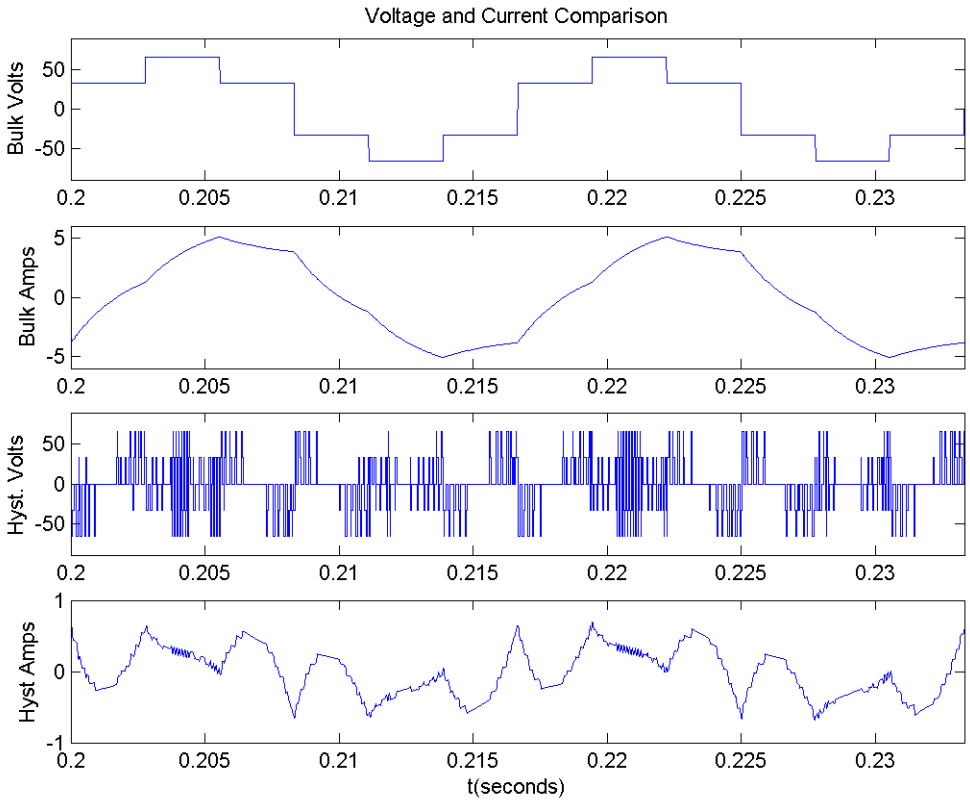

Figure 56. Bulk Inverter (top) and Hysteresis Inverter (bottom) waveform comparison

A small amount of fundamental frequency is present in the hysteresis inverter current wave form. The fundamental has been minimized by manually adjusting the gain and phase-shift correction in the filter assembly. This could easily be corrected with the use of a self-adjusting filter assembly. With the addition of automatic gain-control and automatic phase-correct circuitry, the fundamental content of the hysteresis inverter would be minimized.

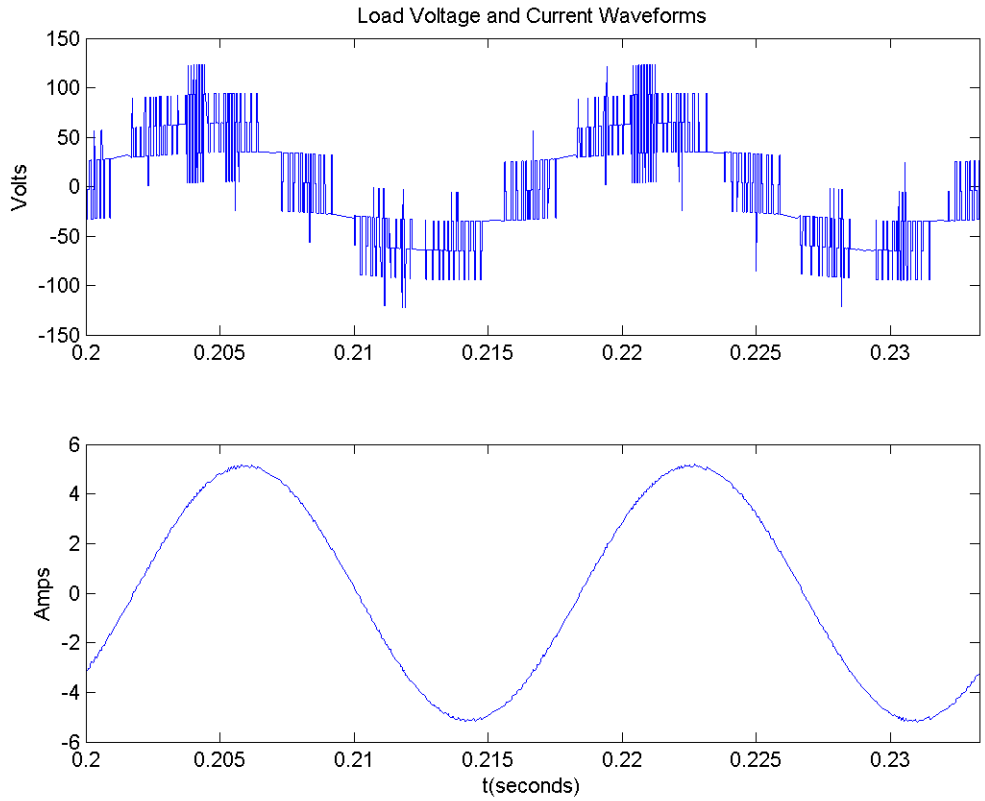

Figure 57. Load Voltage (top) and Current (bottom) Waveforms

The resultant output demonstrates that the new control topology performs quite well in smoothing the load current (Fig. 57). The results of the hybrid controller demonstrate that the hysteresis controlled inverter actively filters the load current to produce a nearly ideal sinusoidal output. The voltage waveform likewise shows a smoother waveform than the bulk inverter alone. The hybrid system model results therefore validate the hysteresis inverter model and provide a reasonable baseline for the laboratory prototype tests.

F. PARK'S TRANSFORM ANALYSIS OF SYSTEM

The model was constructed to allow a system analysis in the dq0 reference frame. Although this is beyond the scope of this research effort, reference frame conversion made the calculations for the dc current into the system much simpler.

The Park's transform is used to simplify the analysis of multi-phase systems. It reduces the complexity of the system and allows analysis of the system in various reference frames: stationary, arbitrary, or (in the case of rotating machines) rotary. The Park's transform is given by [12]:

$$\vec{f}_{qd0} = K_s \cdot \vec{f}_{abc}$$

$$K_s = \frac{2}{3}\begin{bmatrix} \cos(\theta) & \cos\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta + \frac{2\pi}{3}\right) \\ \sin(\theta) & \sin\left(\theta - \frac{2\pi}{3}\right) & \sin\left(\theta + \frac{2\pi}{3}\right) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \tag{4.15}$$

The dq0 analysis block in Figure 40 uses this transformation to obtain the direct and quadrature components of the voltages and currents of both inverters individually and the load voltage and current. From the transformed load elements the average dc current into the system can then be calculated.

By Kirchhoff's current law (KCL) the total dc current into the bridge is given by the following [12]:

$$I_{dc} = i_{adc} + i_{bdc} + i_{cdc} \tag{4.16}$$

Since energy cannot be created in the system, and the power losses are assumed to be minimal in the model, the system power is given as [12]:

$$V_{dc} \cdot I_{dc} = \frac{3}{2}\left(V_{od} \cdot I_{od} + V_{oq} \cdot I_{oq}\right) \tag{4.17}$$

where V_{od} and V_{oq} are the direct and quadrature load voltages and I_{od} and I_{oq} are the direct and quadrature load currents. The dc current into the system can therefore be calculated by:

$$I_{dc} = \frac{3}{2}\frac{\left(V_{od} \cdot I_{od} + V_{oq} \cdot I_{oq}\right)}{V_{dc}} \tag{4.18}$$

Figure 58 shows the plot of dc current versus time. Notice that the dc current to the PCHI is not constant over time. This agrees with the theory presented in Chapter II. The average value of the dc current is 2.95A for a 100V dc input. The average power used by the system is therefore 295W.

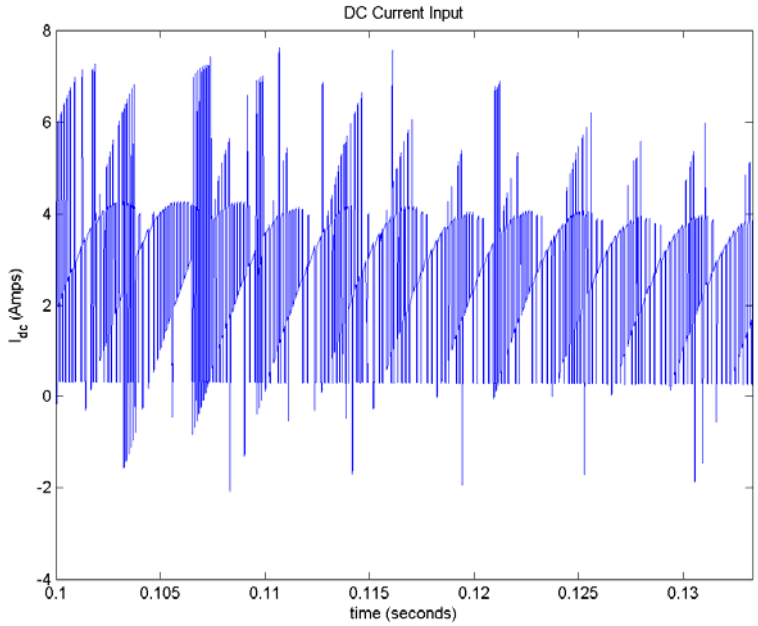

Figure 58. DC Current Calculated (average value 2.95A)

The inverse transform is [12]:

$$f_{abc} = K_s^{-1} f_{dq0}$$

$$K_s^{-1} = \begin{bmatrix} \cos(\theta) & \sin(\theta) & 1 \\ \cos\left(\theta - \frac{2\pi}{3}\right) & \sin\left(\theta - \frac{2\pi}{3}\right) & 1 \\ \cos\left(\theta + \frac{2\pi}{3}\right) & \sin\left(\theta + \frac{2\pi}{3}\right) & 1 \end{bmatrix} \tag{4.19}$$

It is used to convert the dq0 state variables back to the abc-reference frame. This transform was not incorporated in the simulation, but would be required if a dq0-reference control strategy were used. Future research can investigate the use of a dq0

controller. The main disadvantage of the dq0 controller is that it will become much more complex in order to compute the diffeomorphic transformations required to implement it.

G. SUMMARY

This chapter presented the SIMULINK model used to evaluate the new control strategy. The outputs of the bulk controller matched the predicted values of Chapter II. The output of the hysteresis inverter produces a current waveform which precisely cancels the harmonic content of the bulk inverter. A quick harmonic check obtained by summing the currents of all three output phases shows that there is very little harmonic content in the output (Fig. 59). The computer model demonstrates the circuit designed will improve the performance of the PCHI to meet the current harmonic requirement contained in Chapter 10 of the IEEE STD 519 (1999).

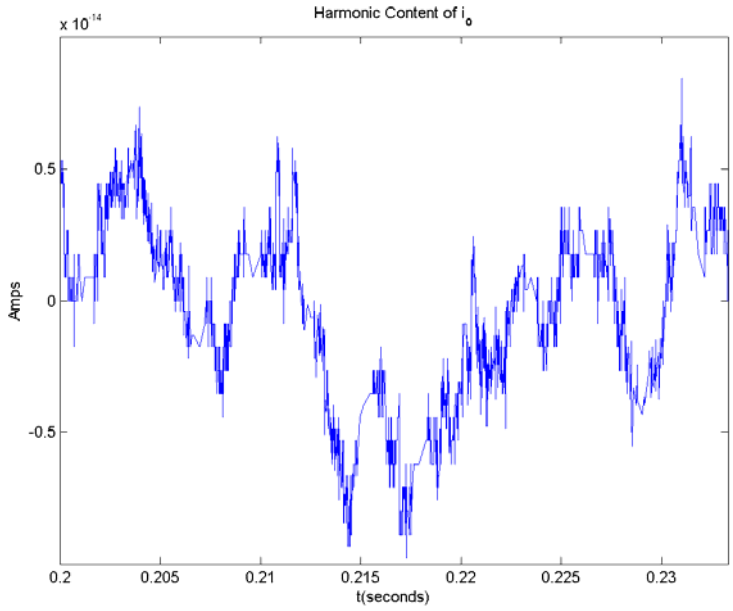

Figure 59. Harmonic Content Test of Load Currents

The model also allows for system analysis in the stationary reference frame using the Park's equation. Future research can use this analysis to design a dq0-reference frame controller which would improve system response. The direct and quadrature waveforms produced by the bulk inverter match the waveforms in Reference [12] further validating that portion of the model.

V. LABORATORY TEST AND CONCEPT VALIDATION

A. OVERVIEW

This chapter presents the laboratory prototype built to validate the new hysteresis controller. The circuits presented in Chapter III were constructed and tested to validate the theory of operation. Circuit performance testing was conducted on the bulk controller, the filter circuit, the sensor circuit, and the hybrid inverter. The bulk and hysteresis inverters were connected in parallel to conduct the final test of the PCHI system. The schematics and pictures of the laboratory setup are recorded in Appendix C.

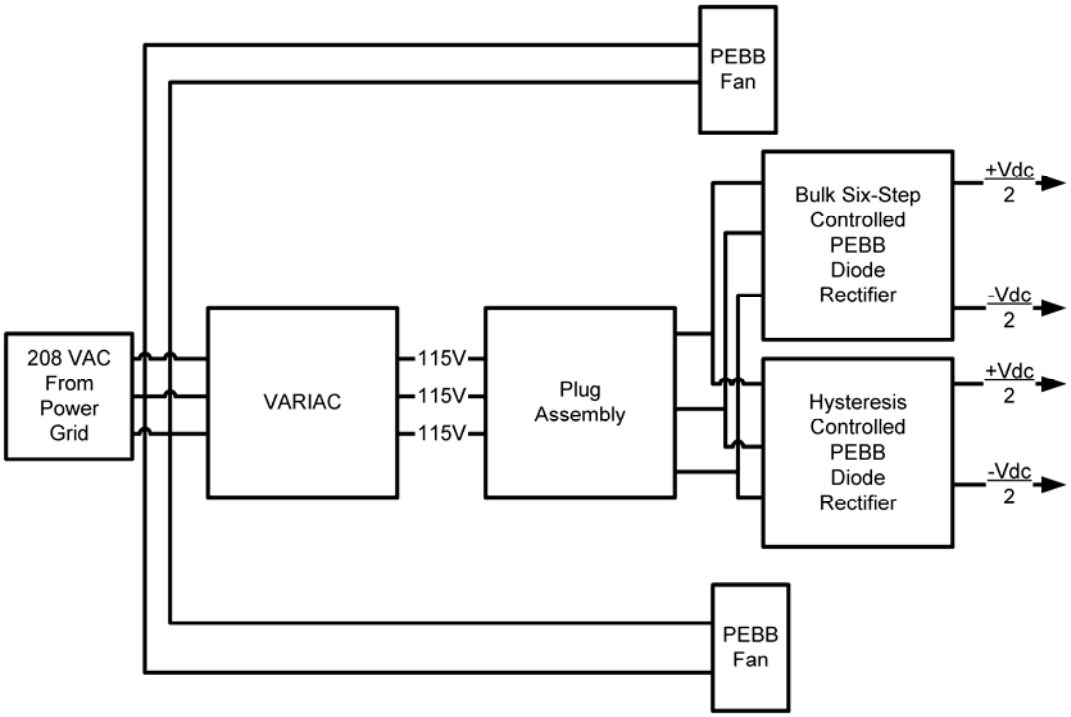

Figure 60. Inverter Power Supply

Power was supplied to the PEBB modules by a three-phase 208V 20A ac circuit in the NPS Power Lab (Fig. 60). The voltage was stepped down to 114V with a variac. The variac output was connected directly to both of the PEBB modules' three-phase diode rectifiers. The PEBB module cooling fans were energized directly from the 208V circuit.

The load used had the characteristics listed in Table 12.

	A	B	C
Load Resistance	10.56Ω	10.33Ω	10.57Ω
Load Inductance	16.4 mH	16.6 mH	16.5 mH
Load Inductor Winding Resistance	0.18Ω	0.21Ω	0.20Ω
Bulk Coupling Inductors	2.56 mH	2.71 mH	2.61 mH
Bulk Coupling Inductor Winding Resistance	0.14Ω	0.10Ω	0.17Ω
Hyst. Coupling Inductors	2.13 mH	2.16 mH	1.89 mH
Hyst. Coupling Inductor Winding Resistance	0.06Ω	0.07Ω	0.05Ω
Bulk DPF (at 60Hz)	0.836	0.825	0.835
Hyst. DPF (at 60Hz)	0.840	0.832	0.842

Table 12. Three-phase Load Characteristics (Bulk Inverter)

As can be seen the load is not perfectly balanced and will cause some error in the system outputs. Three-phase power was provided to the PEBB rectifier bridges to generate a 100V dc bus. Each phase of the bulk inverter was connected to a 2.5 mH coupling inductor and then to the three-phase RL load. The RL load consisted of a series 10Ω resistor and a 20 mH inductor for each phase (Fig. 61). For ease of connection, the bulk inverter was connected to the load via three delta connected isolation transformers.

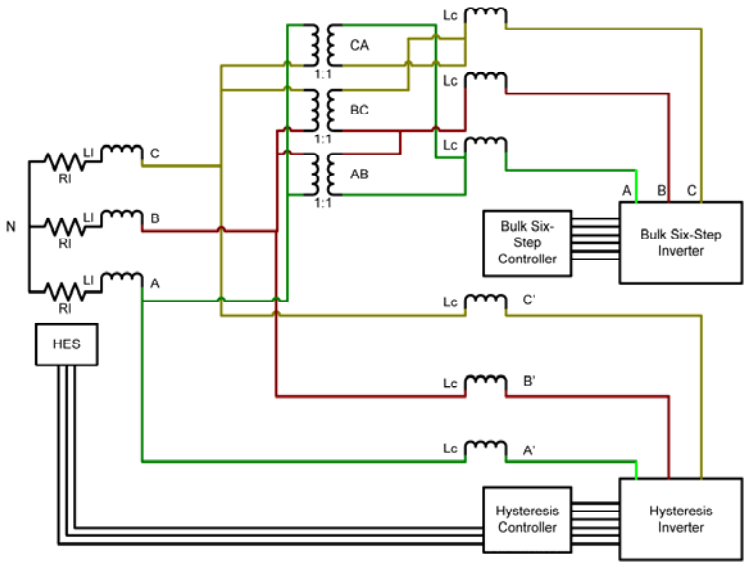

Figure 61. Hybrid System Power Map

B. VSI BUILD AND TEST

The improved bulk six-step controller was tested with a PEBB to determine its performance. A 24V dc power supply powered the control circuitry. The output waveform for each gate signal was a square wave operating at 58.55 Hz (Fig. 62). The relationship between the gate signals is given in Table 13. The signal pattern produced matches that given in Table 3. The maximum and minimum voltages required to trigger the IGBTs were determined experimentally in the lab and match the datasheet specifications for the switches.

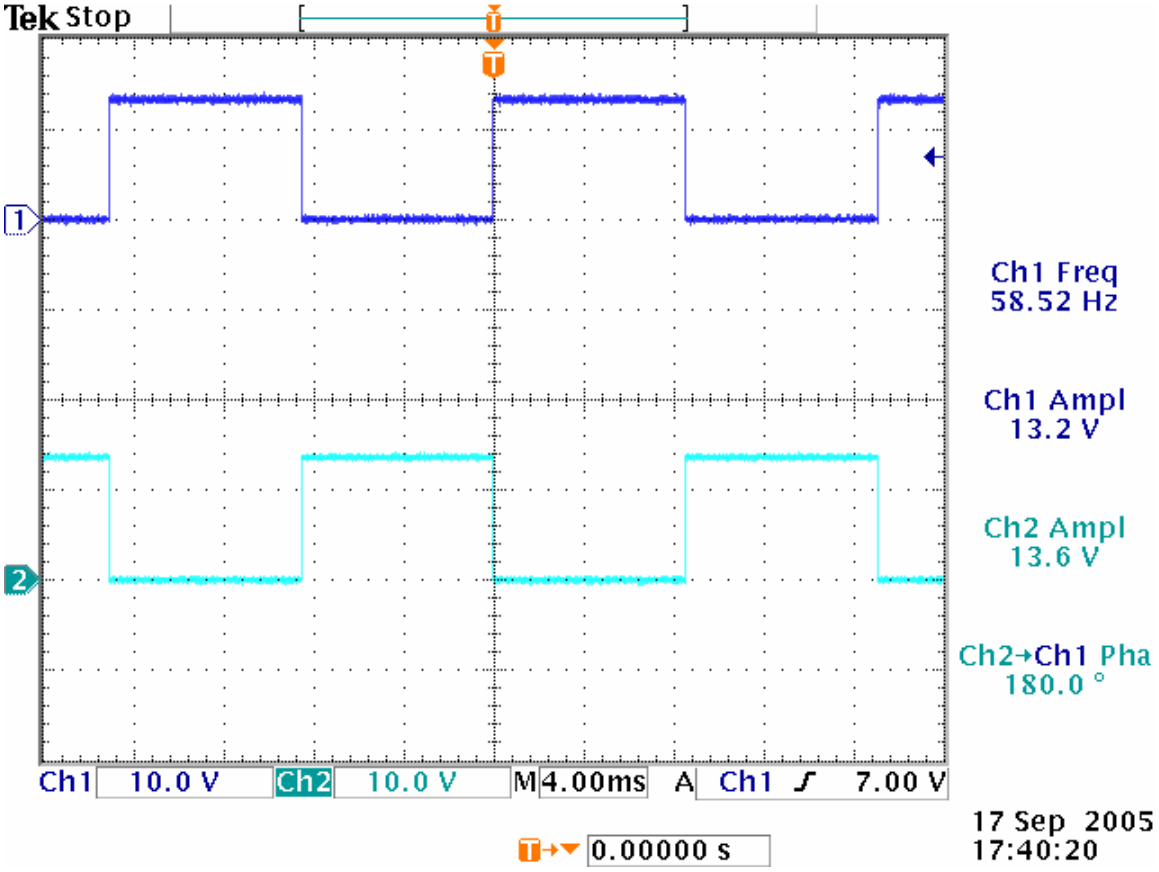

Figure 62. Bulk Six-step Phase A Gate Control Signals: S1 (top) and S2 (bottom)

	A	A!	B	B!	C	C!
Gate Signal	S1	S2	S3	S4	S5	S6
Minimum Voltage (< 5.5V)	0V	0V	0V	0V	0V	0V
Maximum Voltage (>11.5V)	13.4V	13.4V	13.4V	13.4V	13.4V	13.4V
Frequency (Hz)	58.55	58.55	58.55	58.55	58.55	58.55
Phase Shift from S1 (degrees)	0	180	120	-60	-120	60

Table 13. Bulk Six-step Gate Control Signals

The three-phase output waveforms of the bulk inverter match the predicted values of Table 4 and Figure 12 in Chapter II. A 100V 2.5A dc input was applied to the system. The peak voltage of the output is 63 V and the peak current is 3.8A. The observed efficiency of the bulk inverter was 95%.

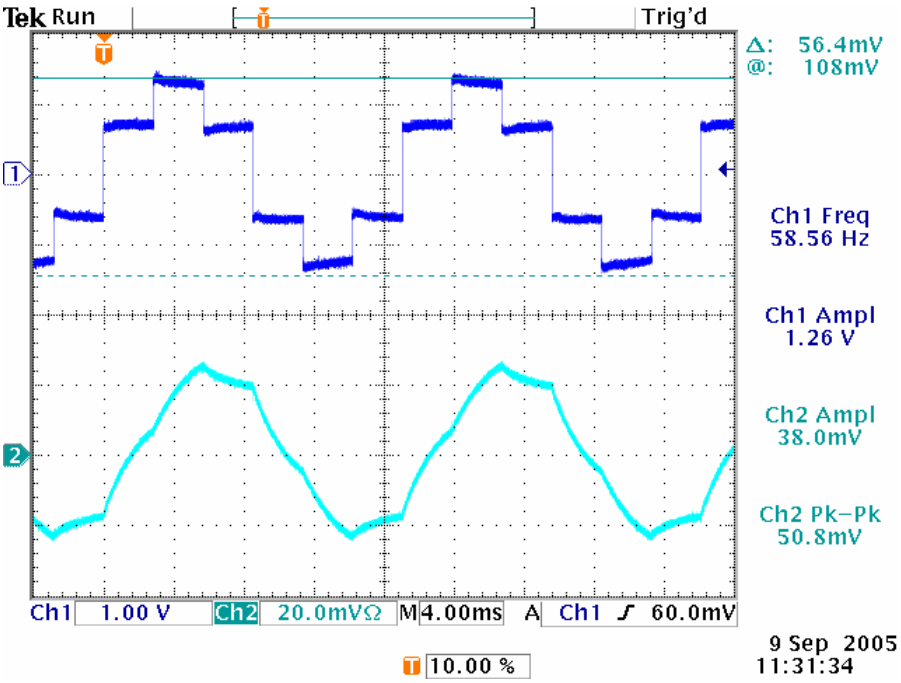

Figure 63. Bulk Inverter Voltage (top) and Current (bottom) Waveforms for Phase A

While the load was not perfectly balanced, the voltages of the other two phases were equivalent to the phase A voltage. The bulk six-step inverter produced the waveforms predicted by the SIMULINK model (Fig. 63).

The bulk inverter was connected to the load as shown in Figure 61. The resultant output demonstrated a slight loss in power efficiency, but the phase voltages and currents were acceptable for testing the hybrid inverter (Fig. 64). The harmonic content of the load current contains no even harmonics or third harmonic multiples (Fig. 65). The highest harmonic is -22 dB below the fundamental and the calculated THD is 7.742%. The small (-42 dB) third harmonic observed is caused by the unbalanced load and is sufficiently low to not interfere with the hybrid prototype experiment.

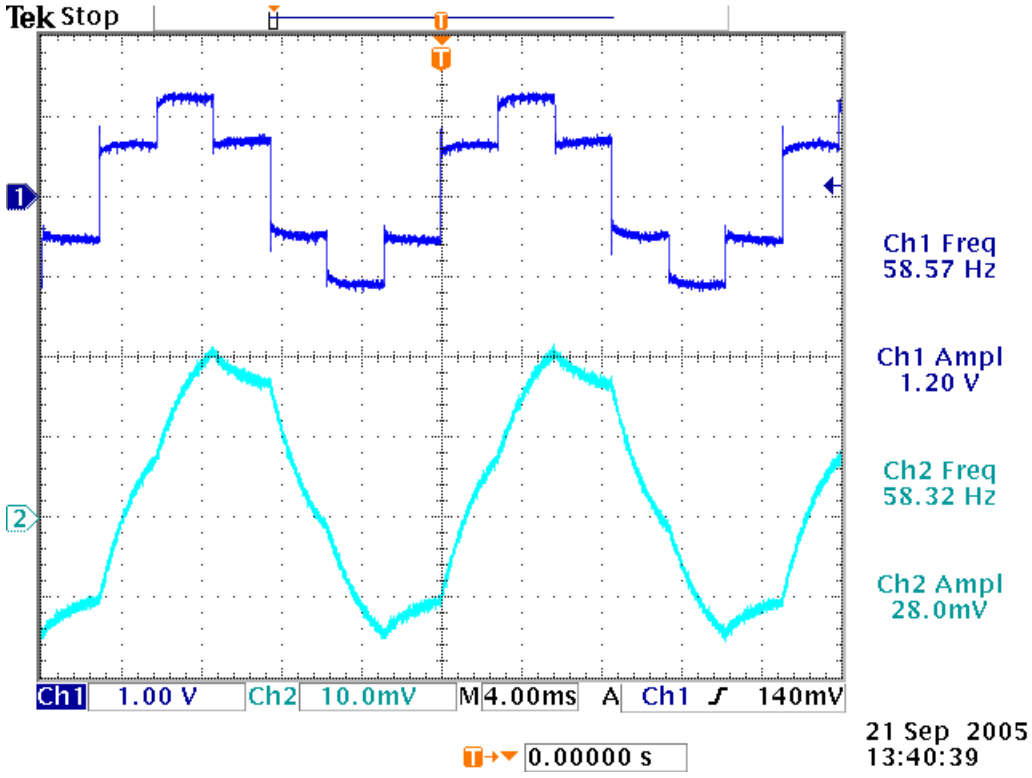

Figure 64. Bulk Inverter Output through the Delta-Connected Transformers

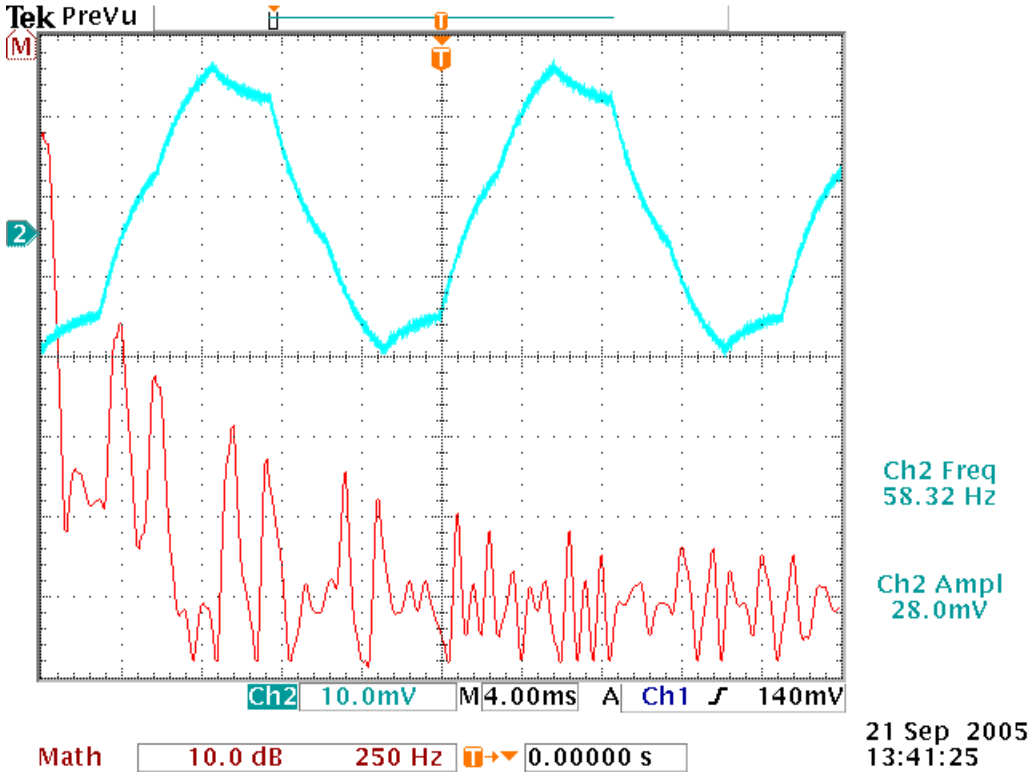

Figure 65. Bulk Inverter Load Current Harmonic Content.

C. FILTER TEST

The three-phase filter design was tested using the output from the Hall Effect sensors. The sensor output gain was fully adjustable. The output of the LPF was phase shifted -28.6° with a gain of 1.7 (Fig. 66). This validates the filter design of Chapter III. The small percentage of error is caused by the variations in the capacitor and resistor values used to construct the filter.

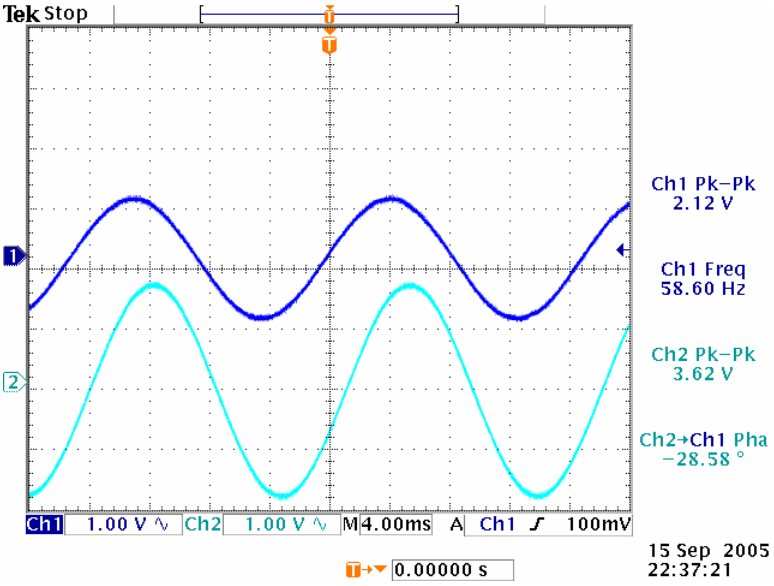

Figure 66. LPF phase shift and gain

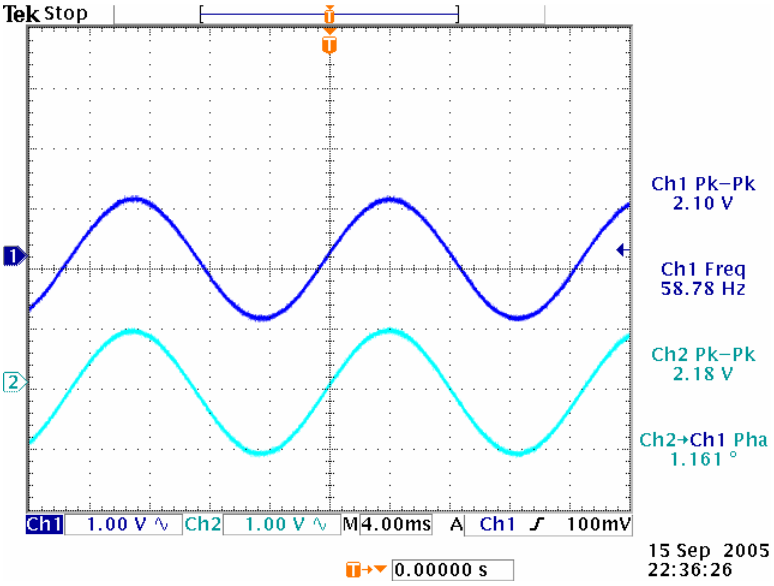

Figure 67. Phase and Gain Corrected Output

The phase correction and gain correction circuitry allowed the filter output to be precisely matched to the input (Fig. 67). All three filters were calibrated using a 60 Hz sinusoidal signal to match the filter output with the input. The calibrated filter was used to condition the load current waveform and to generate the reference waveform for the hysteresis circuit (Fig. 68).

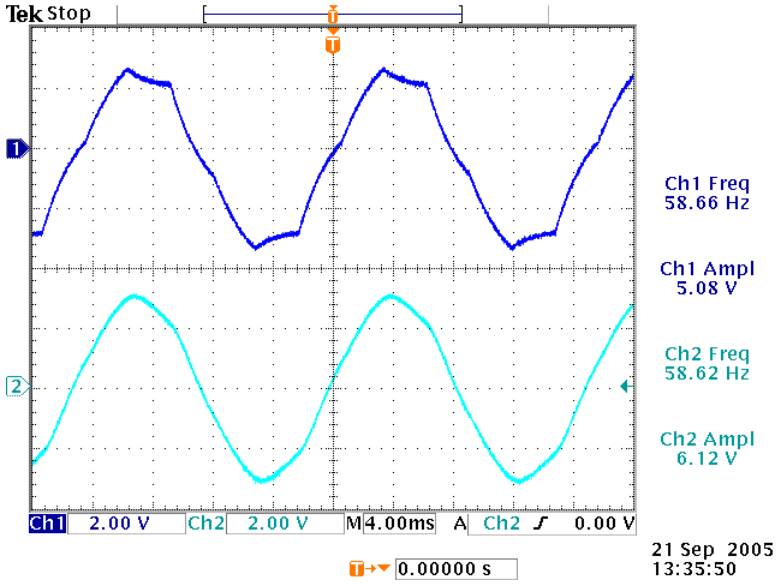

Figure 68. Load Current (top) and Filtered Reference Waveform (bottom)

The harmonic content of the reference waveform is much lower than the load current waveform (Fig. 69). The highest harmonic observed is the fifth harmonic at -34 dB down from the fundamental. All three filters performed satisfactorily for use in the prototype hysteresis controller.

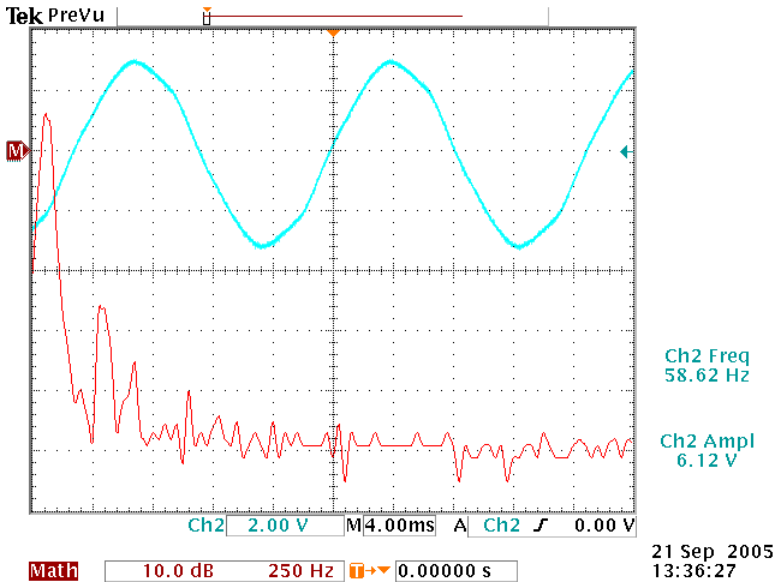

Figure 69. Bulk Inverter Generated Reference Waveform Harmonics

D. HYSTERESIS CIRCUIT TEST

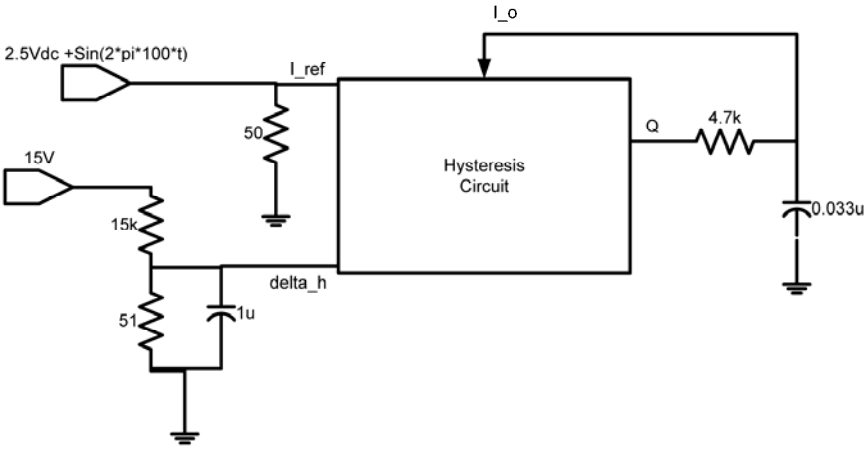

Figure 70. Hysteresis Test Circuit

The hysteresis circuit for each phase was tested using the circuit shown above (Fig. 70). The resulting output demonstrates the switching capability of the hysteresis circuit (Fig. 71). The maximum frequency observed was 135 kHz which is well above the 13 kHz hysteresis error signals expected. This is far in excess of the frequencies expected, but it is a dramatic demonstration of the hysteresis circuit's switching capability. All three phases produced identical results. The single-phase test validates the switching frequency findings of References 9 and 10 which were restated in Chapter II.

The maximum observed switching frequency occurs at the maxima and minima of the reference signal and the minimum switching rate occurs at the zero crossings.

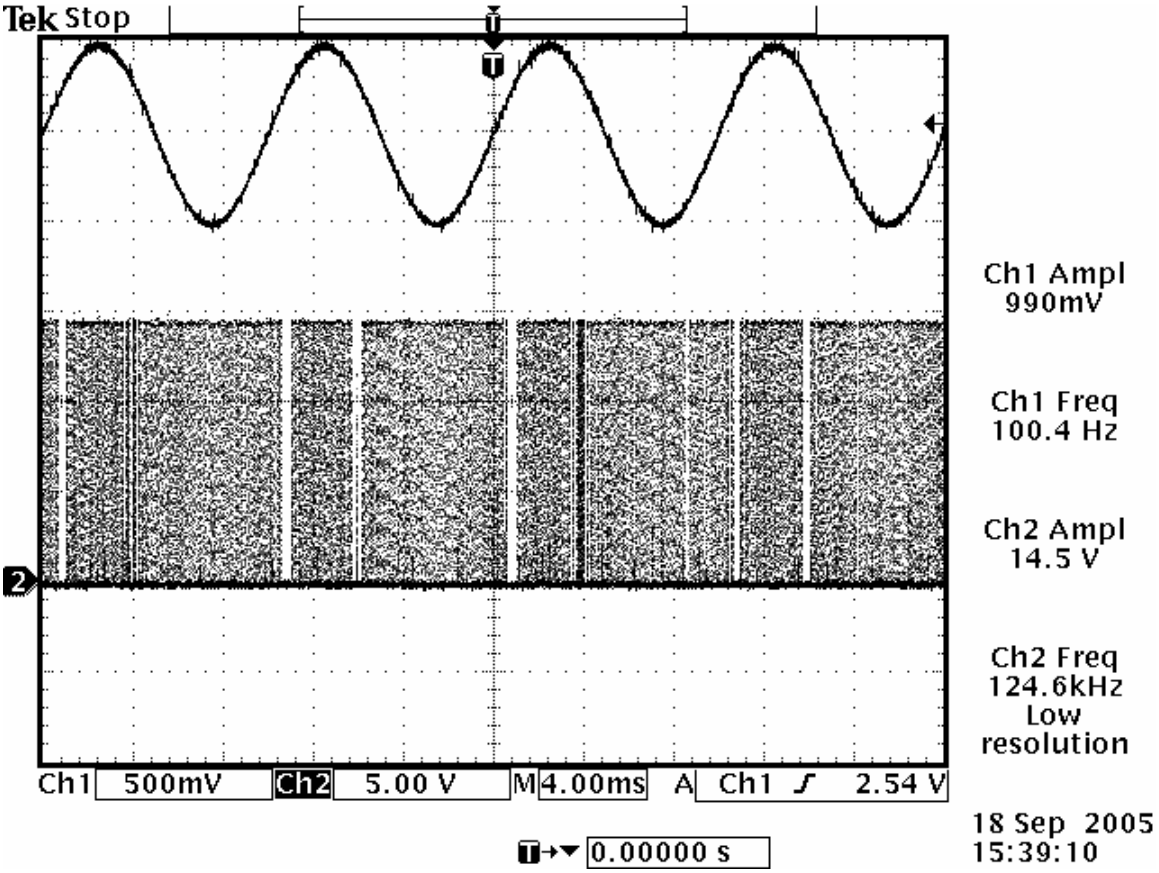

Figure 71. Hysteresis Circuit Test: top – Reference Waveform, bottom – Error signal (Q)

E. OPEN-LOOP TEST OF HYSTERESIS CONTROLLER

The Hall-effect sensor circuit and the filter circuit were coupled to the hysteresis circuit to demonstrate an open loop system test. The expectation is that a comparison of the raw bulk inverter load current with the conditioned reference waveform would generate error signals from the hysteresis circuit (Fig. 72). When the bulk inverter output current is greater than the upper tolerance band of the reference wave, a gate signal (Q!) should latch the lower switch in the corresponding half-bridge in the hysteresis inverter. Likewise a violation below the tolerance band should create a gate signal (Q) to latch the upper switch. The results of this test are shown in Figures 73 and 74. The gate signals validate the logic provided in Chapter II. All three phases gave identical results.

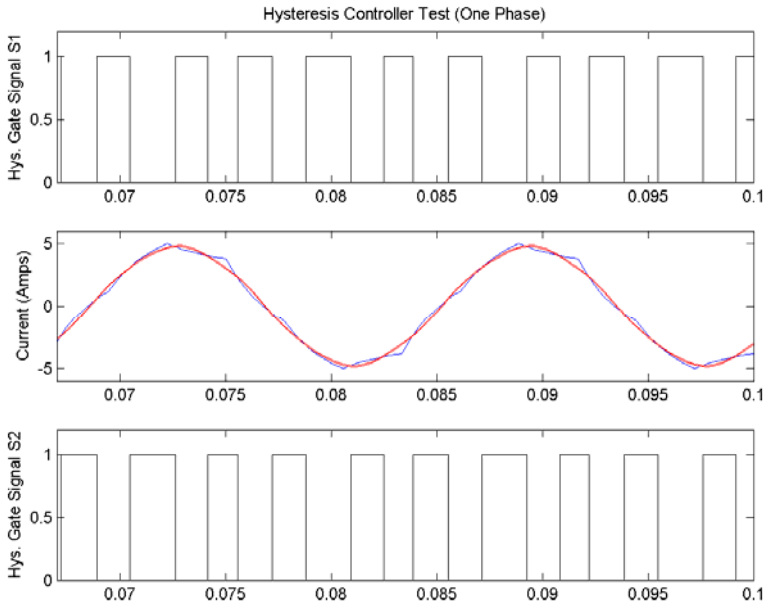

Figure 72. Hysteresis Controller Single Phase Gate Signals (S1 and S2)

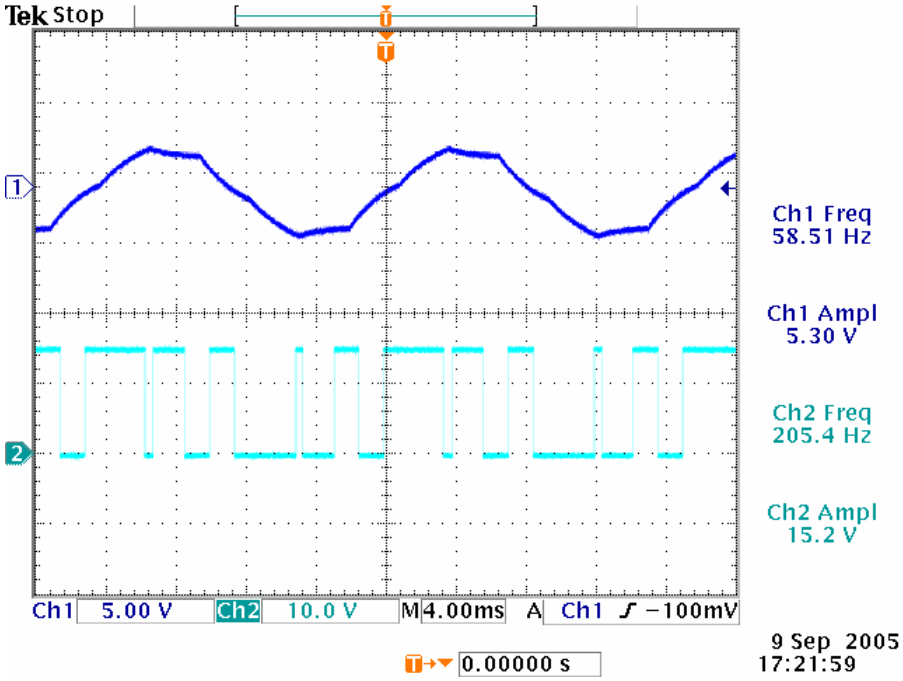

Figure 73. Hysteresis Generated Gate Control Signal (S1)

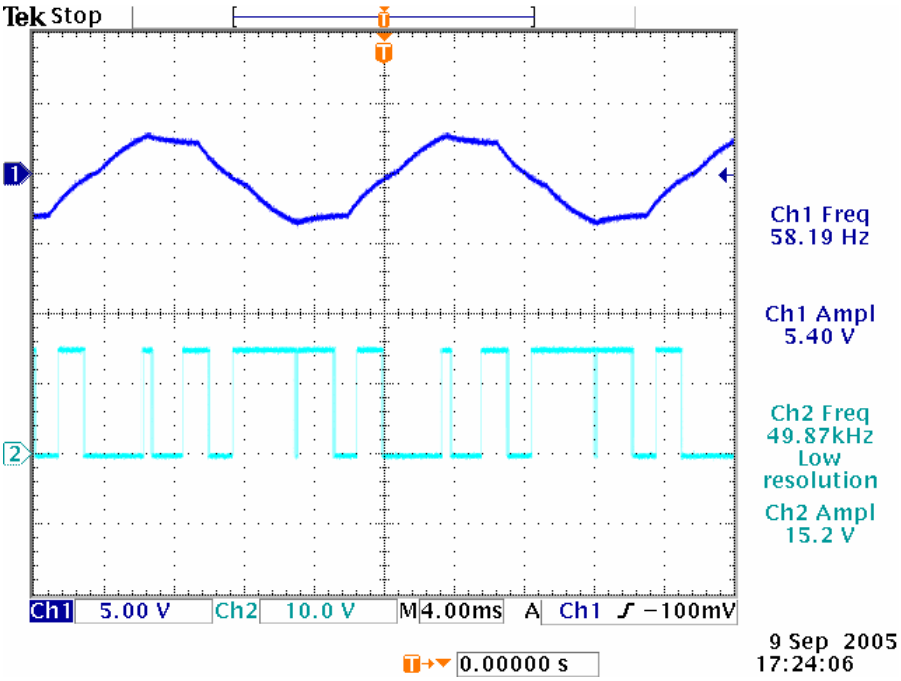

Figure 74. Hysteresis Generated Gate Control Signal (S2)

F. COUPLING INVERTERS TO LOAD

The final test of the system required the coupling of the bulk inverter and the hysteresis inverter as shown in Figure 61. All three phases of both inverters contained 2.5 mH series coupling inductors. The outputs of the bulk coupling inductors were sent to three isolation transformers to ensure that there was no zero-sequence current in the system. The transformers' primary and secondary windings were delta connected and then sent to a wye-connected load. The transformers were designed for 60Hz operation so some power loss is expected from the high frequency operation of the hysteresis controlled inverter. The outputs of the hysteresis inverter were directly coupled to the load to actively filter the harmonic content of the current.

The results show a dramatic improvement in the load current (Fig. 75). The peak output voltage observed was 64V and the output current was 6.48A. The THD of the load current is improved to 1.8% with the highest harmonic at -35.2 dB below the fundamental (Fig. 76). The reference waveform also shows marked improvement over the initial reference shape produced (Figs. 77 and 78). The highest harmonic observed is the third harmonic at -36 dB below the fundamental.

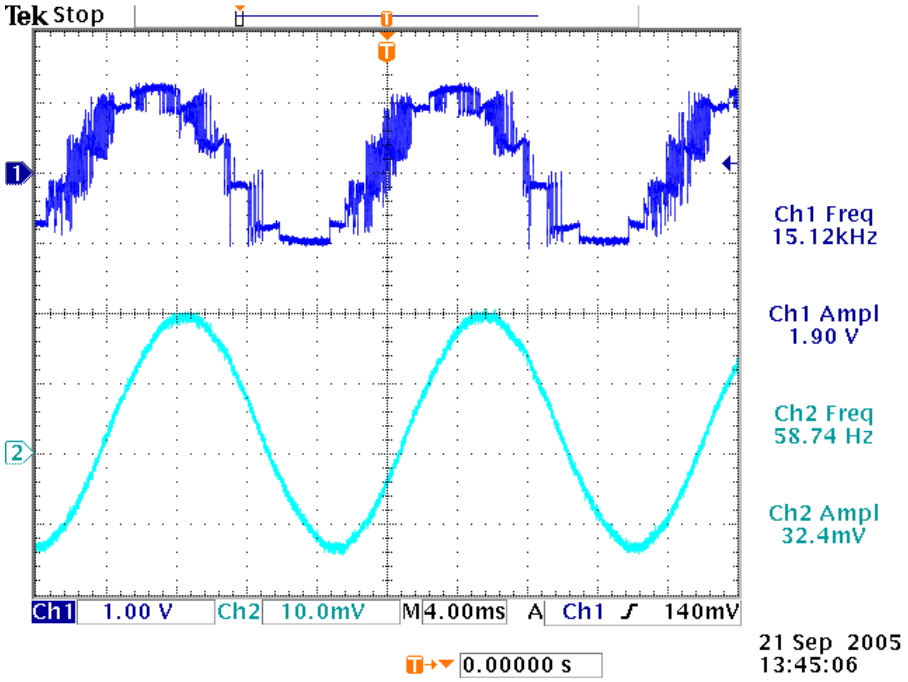

Figure 75. PCHI Load Waveforms: Load Voltage (top), Load Current (bottom)

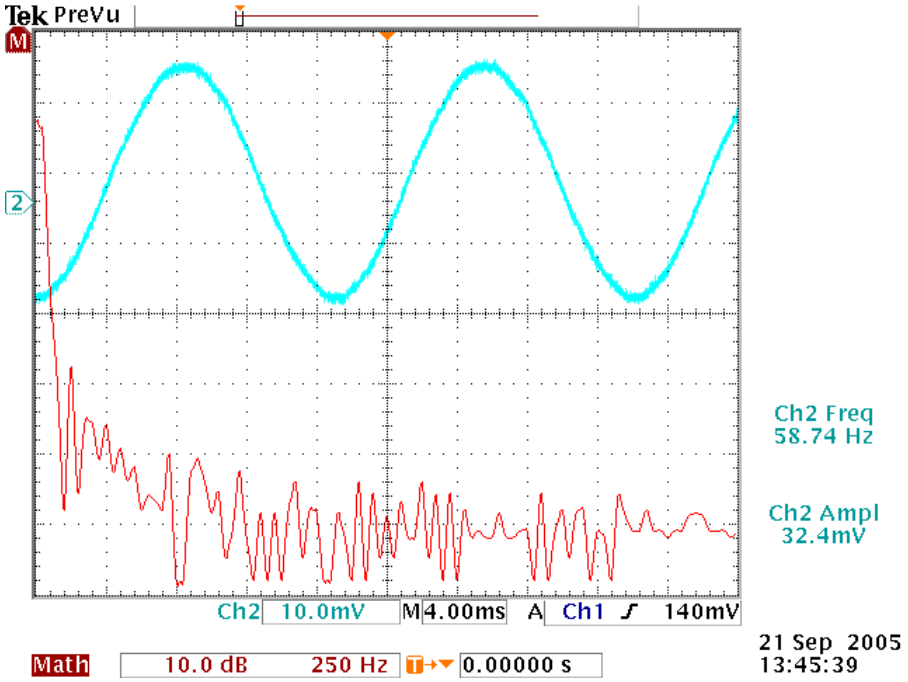

Figure 76. PCHI Load Current Harmonic Content

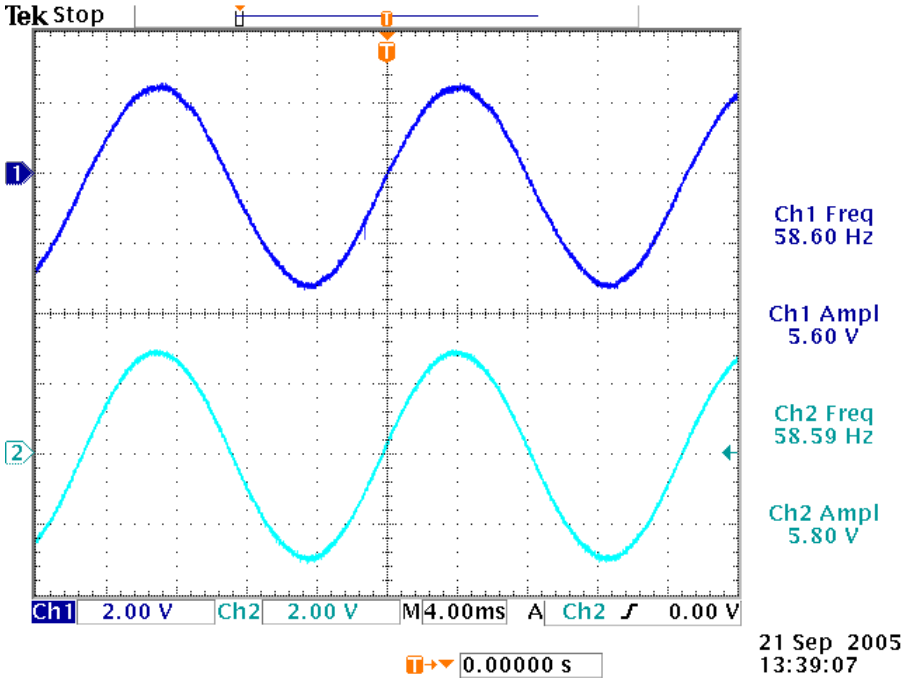

Figure 77. PCHI Load Current (top) and Improved Reference Waveform (bottom)

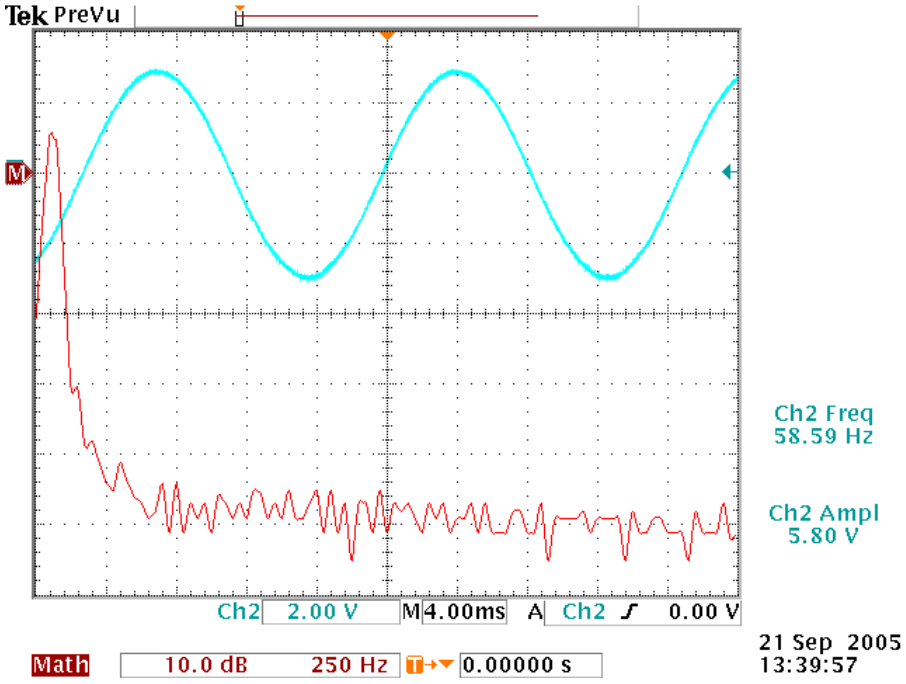

Figure 78. PCHI Reference Waveform Harmonic Content

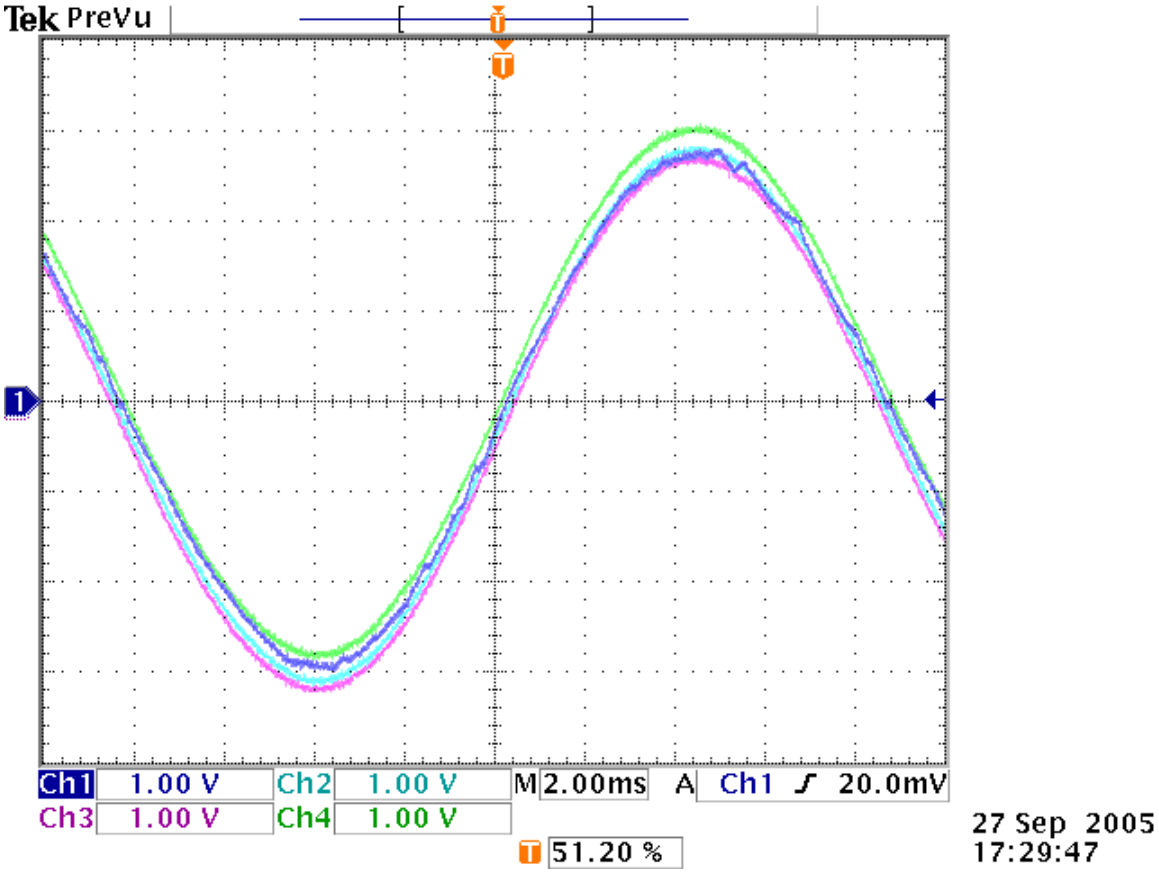

Figure 79. Load Current comparison with the Reference Signal and the Tolerance Band

A comparison of the load current with the tolerance band demonstrates the effectiveness of the hysteresis controller in maintaining the output within the tolerance bands (Fig. 79). The upper and lower sine waves mark the boundaries of the tolerance band, the middle sine wave is the reference signal, and the jagged waveform is the sensed load current. No boundary excursions were observed for the PCHI system. The main sources of the harmonic distortion observed include the unbalanced three-phase load, the interaction between the hysteresis inverter and the three 60Hz transformers, and slight filter mismatches. The highest switching frequency observed by the hysteresis controller is approximately 5 kHz which indicates that the multi-phase switching frequency is significantly less than that required for single-phase operation (Figs. 80 and 81). This approximate factor of three reduction may be related to the pseudo-interleaving of the phases of the three-phase system. However, this analysis will need to be the topic of a future research effort.

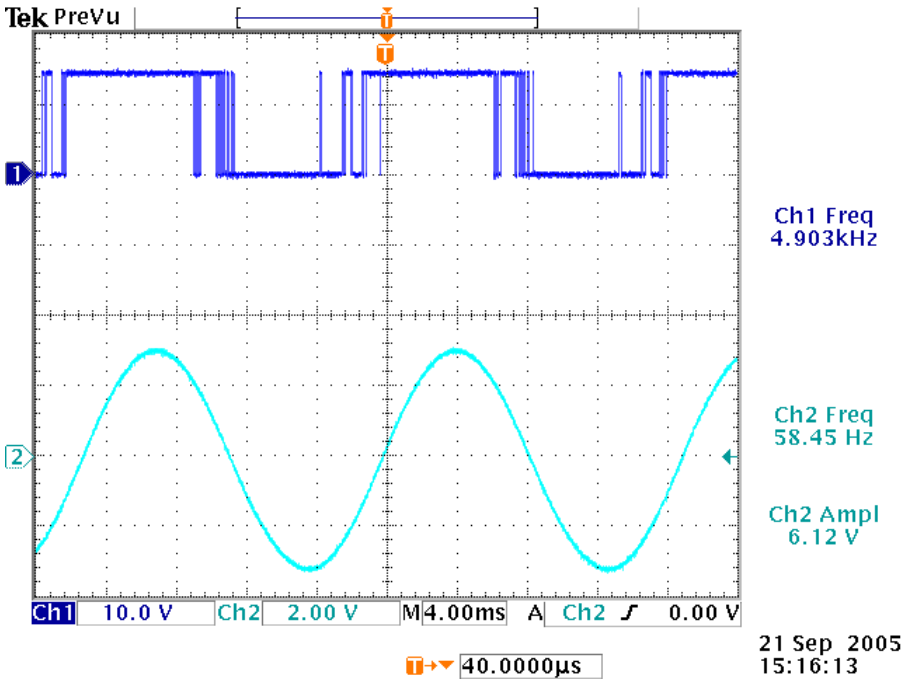

Figure 80. Hysteresis Controller Error Signal (Gate Signal S1)

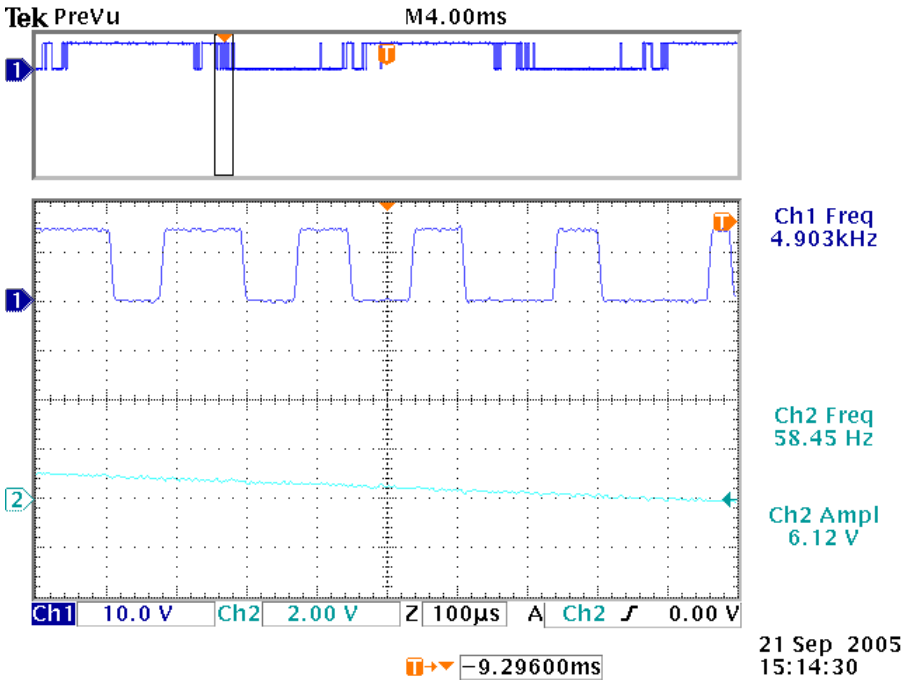

Figure 81. Hysteresis Controller Maximum Switching Frequency (Phase A)

G. LABORATORY RESULTS

The PCHI system built in the lab performed quite well. The bulk inverter current THD was reduced from 7.74% to 1.81% (Figs. 82 and 83, Tables 14 and 15). There was a significant increase in the low harmonic noise due to the interaction between the hysteresis inverter output and the delta connected transformers providing the bulk-inverter output. The hybrid inverter system was tested by coupling the bulk-inverter directly to the load. This noticeably reduced the quality of the hybrid current waveform. The best system performance was achieved with the bulk inverter delta connected to the load via the three-isolation transformers. The IEEE Std. 519 current harmonic limit is 2.5%. The PCHI system meets the final objective by 0.7% and is a 1.8% improvement over the previous thesis.

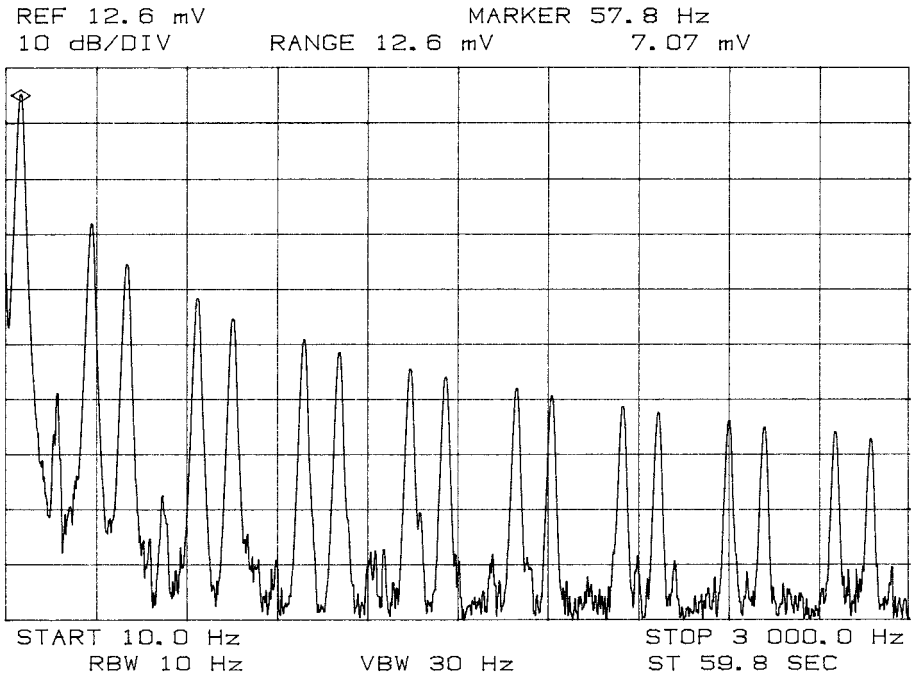

Figure 82. Bulk Inverter Harmonics

Harmonic	Frequency	Voltage	Level	Output Lvl	Square	Ratio
1	60	7.15	1.00E-03	0.00715	5.11225E-05	1
3	177.4	14.4	1.00E-06	0.0000144	2.0736E-10	4.05614E-06
5	294	489	1.00E-06	0.000489	2.39121E-07	0.004677412
7	410.6	216	1.00E-06	0.000216	4.6656E-08	0.000912631
11	646.8	105	1.00E-06	0.000105	1.1025E-08	0.000215658
13	763.4	68.3	1.00E-06	0.0000683	4.66489E-09	9.12493E-05
17	996.7	43.6	1.00E-06	0.0000436	1.90096E-09	3.71844E-05
19	1113.3	33.5	1.00E-06	0.0000335	1.12225E-09	2.19522E-05
23	1349.5	24	1.00E-06	0.000024	5.76E-10	1.12671E-05
25	1466.1	19.9	1.00E-06	0.0000199	3.9601E-10	7.7463E-06
29	1699.3	15.5	1.00E-06	0.0000155	2.4025E-10	4.6995E-06
31	1815.9	13.3	1.00E-06	0.0000133	1.7689E-10	3.46012E-06
35	2052.1	10.8	1.00E-06	0.0000108	1.1664E-10	2.28158E-06
37	2168.7	9.32	1.00E-06	0.00000932	8.68624E-11	1.6991E-06
41	2402	8.21	1.00E-06	0.00000821	6.74041E-11	1.31848E-06
42	2518.6	6.68	1.00E-06	0.00000668	4.46224E-11	8.72852E-07
46	2754.8	6.45	1.00E-06	0.00000645	4.16025E-11	8.13781E-07
48	2871.4	5.43	1.00E-06	0.00000543	2.94849E-11	5.7675E-07
					Sum of Ratios:	0.005994879
					Square Root:	0.077426607
					THD(%)	**7.742660707**

Table 14. Experimental Bulk-Inverter Current Harmonics Observed in Figure 81

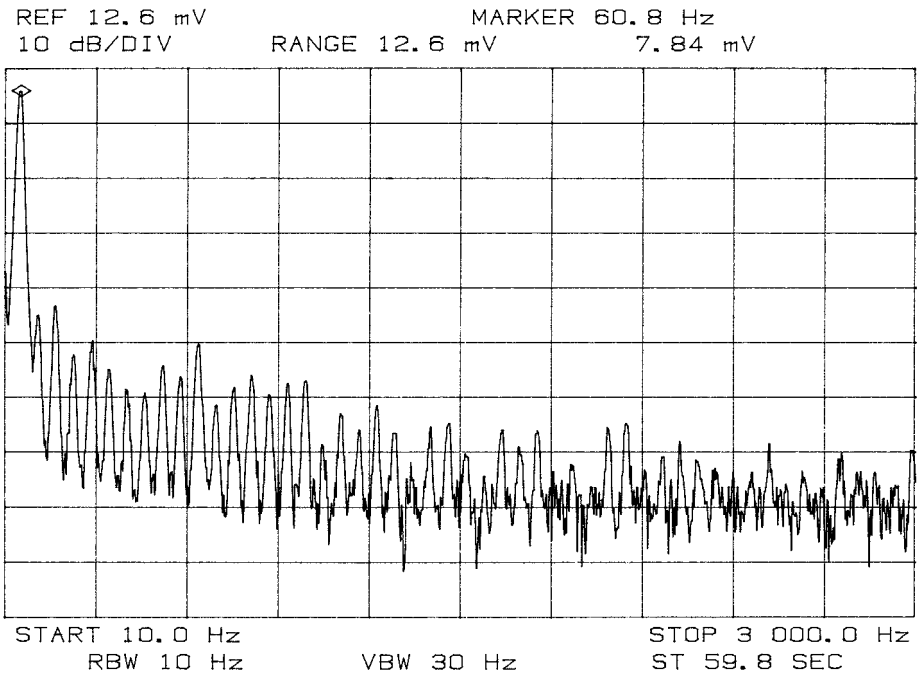

Figure 83. PCHI Harmonics

Harmonic	Frequency	Voltage	Level	Output Lvl	Square	Ratio
1	60.8	7.84	1.00E-03	0.00784	6.14656E-05	1
2	120.6	70.7	1.00E-06	0.0000707	4.99849E-09	8.13217E-05
3	177.4	85	1.00E-06	0.000085	7.225E-09	0.000117545
4	237.2	30.2	1.00E-06	0.0000302	9.1204E-10	1.48382E-05
5	300	41.2	1.00E-06	0.0000412	1.69744E-09	2.76161E-05
6	353.8	22.6	1.00E-06	0.0000226	5.1076E-10	8.30969E-06
7	407.6	14.8	1.00E-06	0.0000148	2.1904E-10	3.56362E-06
8	470.4	13.6	1.00E-06	0.0000136	1.8496E-10	3.00916E-06
9	530.2	24.2	1.00E-06	0.0000242	5.8564E-10	9.52793E-06
10	587	19.3	1.00E-06	0.0000193	3.7249E-10	6.06014E-06
11	646.8	38.4	1.00E-06	0.0000384	1.47456E-09	2.399E-05
12	706.6	10.7	1.00E-06	0.0000107	1.1449E-10	1.86267E-06
13	763.4	15.1	1.00E-06	0.0000151	2.2801E-10	3.70955E-06
14	820.2	19.9	1.00E-06	0.0000199	3.9601E-10	6.44279E-06
15	877.1	13.2	1.00E-06	0.0000132	1.7424E-10	2.83476E-06
16	939.8	16.6	1.00E-06	0.0000166	2.7556E-10	4.48316E-06
17	999.6	17.6	1.00E-06	0.0000176	3.0976E-10	5.03957E-06
19	1113.3	8.8	1.00E-06	0.0000088	7.744E-11	1.25989E-06
21	1232.9	10.6	1.00E-06	0.0000106	1.1236E-10	1.82801E-06
25	1469.1	7.24	1.00E-06	0.00000724	5.24176E-11	8.52796E-07
27	1582.7	2.37	1.00E-06	0.00000237	5.6169E-12	9.13828E-08
30	1809.9	2.6	1.00E-06	0.0000026	6.76E-12	1.0998E-07
31	1869.7	3.02	1.00E-06	0.00000302	9.1204E-12	1.48382E-07
34	2049.1	7.24	1.00E-06	0.00000724	5.24176E-11	8.52796E-07
37	2198.6	2.21	1.00E-06	0.00000221	4.8841E-12	7.94607E-08
39	2342.2	2.78	1.00E-06	0.00000278	7.7284E-12	1.25735E-07
40	2402	2.57	1.00E-06	0.00000257	6.6049E-12	1.07457E-07
41	2461.8	2.57	1.00E-06	0.00000257	6.6049E-12	1.07457E-07
42	2518.6	4.67	1.00E-06	0.00000467	2.18089E-11	3.54815E-07
44	2629.2	2.63	1.00E-06	0.00000263	6.9169E-12	1.12533E-07
46	2754.8	3.46	1.00E-06	0.00000346	1.19716E-11	1.94769E-07
48	2865.4	2.57	1.00E-06	0.00000257	6.6049E-12	1.07457E-07
					Sum of Ratios:	0.000326487
					Square Root:	0.018068964
					THD(%)	**1.806896376**

Table 15. PCHI Current Harmonics Observed in Figure 82

H. SUMMARY

Differences that were observed between theory and actual laboratory results were caused by the unbalanced load, the width of the hysteresis band, filter mismatches, and the 60Hz (low-frequency) transformer. The load was left slightly unbalanced to replicate the "real-world" application of the controller. Other areas of the controller could be changed to improve the fidelity of the load current, as listed below.

First, the hysteresis band can be reduced to a smaller value by replacing components in the hysteresis circuit. To create the hysteresis tolerance band, 0.051V is added and subtracted to the 6V reference wave to create the tolerance band. The resultant band was approximately 1.7%. If the tolerance band were reduced to 1%, the load current fidelity would be improved. The switching frequency of the hysteresis controller would increase from the 5 kHz observed. The 20 kHz PEBB switching limit will allow a smaller tolerance band. Further research could investigate tolerance band versus maximum switching frequency.

Second, the three filters can be tuned to optimize the output. Once the filters were installed in the circuit they were not adjusted further to match either the unbalanced load or to correct for the actual bulk inverter operating frequency. Manually tuning the filters would be a time consuming process with the filter topology used in this thesis. Future research should focus on replacing the filter with one that detects the bulk inverter output frequency, optimizes the cut-off frequency, and automatically phase and gain corrects the LPF output. This will ensure that a nearly idealized reference waveform is constantly phase and gain locked to the load current.

Third, the antagonistic action between the hysteresis inverter and the bulk inverter through the coupling transformers adds unwanted broadband noise (Figs. 81 and 82). An optimization of the reactances in the circuit will need to be analyzed to correct this phenomenon. The bulk inverter and hysteresis inverter interface may require an additional filter to improve the fidelity of the hybrid inverter output current. Even without correction the overall load current THD improvement is exceptional

Fourth, the use of the dq0-reference frame would simplify the control topology and enable the use of an FPGA more easily. The conversion to the stationary dq0-

reference frame would create a more robust and responsive controller. The FPGA construct simplifies the circuit required to implement the complex mathematics required to transform the system from one reference frame to another while automatically adjusting the system performance and filter parameters to the bulk-inverter system.

The PCHI prototype performance validates the use of a hysteresis controlled inverter to filter the load current generated by a bulk inverter (Fig. 84). The resultant load current demonstrates the reduction in harmonic content from the raw bulk inverter current. This reinforces the findings of Reference 10. The new control method reduced the THD of the load current to 1.8% which exceeded the IEEE Std. 519 (1999) limit of 2.5%.

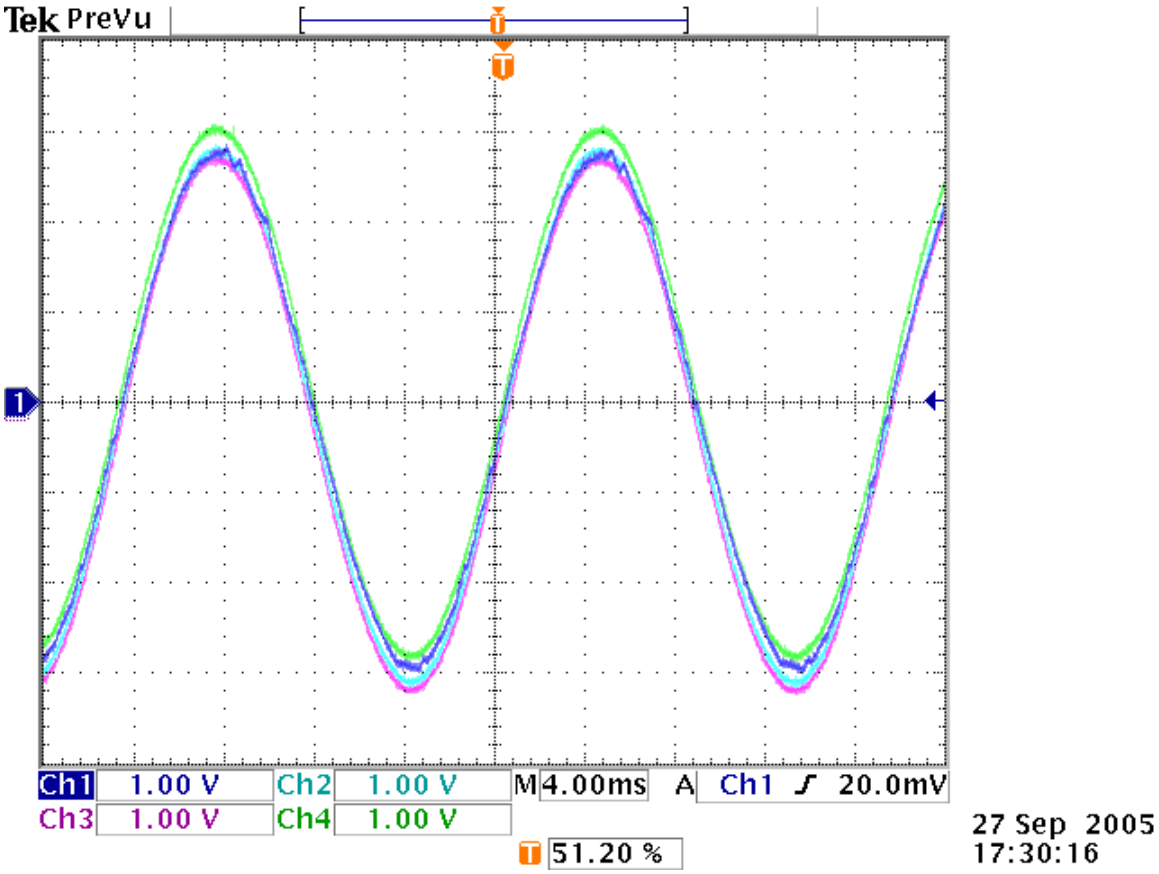

Figure 84. Hysteresis Control of Load Current (Phase A)

VI. CONCLUSION

A. REVIEW OF RESEARCH GOALS

All of the goals were met. Specific goals of this thesis are as follows:

- Simplify the six-step inverter controller design for the VSI. Provide variable operational frequency capability.
- Modify the Hysteresis controller to provide a control signal delay. This allows the IGBT driver cards to power up before they receive gating signals.
- Design a circuit to extract a reference sine wave which is phase-locked to the system output frequency. Ultimately this design will allow variable frequency operation of the system.
- Utilize commercially available Semikron PEBB as the power section for both the VSI and the CSI.
- Develop equations and optimize hysteresis bandwidth to produce the best (highest quality) output current in order to meet or exceed IEEE Standard 519 (1999) requirements for three-phase half-bridge inverters. Total Harmonic Distortion (THD) of 2.5% or better desired.
- Model the system using SIMULINK to provide proof of concept.
- Couple the bulk six-step inverter and the hysteresis controlled inverter to create a hybrid parallel inverter system.
- Test the hybrid system to determine the optimal operating set-point. Increase the power output of the system.

Successful testing of the prototype hybrid hysteresis inverter validates the efficacy of the system for use in powering small and medium sized motor loads with the associated PEBB.

B. FOLLOW-ON RESEARCH

The tests conducted in this thesis were performed using a single system frequency. The PCHI needs to be modified to permit variable frequency operation. The hysteresis controller must detect the bulk inverter frequency and generate the reference waveforms over a range of frequencies. The ideal filter topology would automatically optimize the LPF for the system frequency and automatically correct the gain and the phase shift of the adjustable low-pass filter.

Because the system was able to be modeled in SIMULINK, the hysteresis controller could be built using an FPGA. Several changes are needed to facilitate the conversion. The filter used in this thesis would have to be converted from the continuous form to a discrete form. The pulse generators used in the bulk controller may also need to be replaced. An FPGA based controller would simplify the construction of the variable frequency operation system. The FPGA based system would ensure that the three filters would be frequency locked to the system frequency. The filters would be identical and automatically set by one frequency source which solves the problem of balancing the FPGA filters.

A dq0-reference frame controller should be designed using the dq0 transformations presented in Chapter IV. The conversion to the stationary dq0 reference frame would provide a more responsive and robust controller. The FPGA construct opens the possibility of programming a chip to perform the complex mathematics to transform from one reference frame to another while automatically adjusting the filter parameters.

C. MILITARY APPLICATIONS

The spread spectrum nature of the modulation and the uncertainty (random nature) of a switching event, make this system ideal for stealth operation. When coupled with a variable frequency bulk inverter, shipboard loads can be driven at the most efficient frequency of operation and reduce the predominately 50Hz, 60Hz and 400Hz tonals onboard allied warships. An ideal application would be to replace the dc-to-ac motor-generator sets in the fleet. These are maintenance intensive and are a significant life-cycle cost-driver. A solid-state power converter would reduce the maintenance

requirements of the system and would significantly reduce the life-cycle costs of the platform in the long run. The significant initial investment would pay for itself many times over in reduced maintenance over a thirty year life span.

D. CONCLUSION

All of the stated objectives were met. The six-step controller was simplified and the new design performed well at approximately 60 Hz. Both the modified hysteresis controller and the bulk controller were able operate with the Semikron PEBBs. The hysteresis controller filter produced three nearly ideal sinusoids from the sensed load current to generate reference waveforms for use by the hysteresis circuit of Reference 9. The single phase hysteresis controller test demonstrated that the switching frequency relationship with the reference signal was valid.

The SIMULINK model demonstrated that the new control strategy was valid and would potentially reduce the harmonic content of the load current. Finally the laboratory constructed PCHI provided solid proof that the hysteresis controlled inverter is a very capable active filter for the bulk inverter. The observed PCHI-generated load current THD was 1.81% which exceeds the IEEE Std. 519 (1999) limit of 2.5%. The PCHI system constructed in this thesis provides a simple method to filter the harmonic content from an inductive load. This thesis proves that existing technology can be used to produce high-fidelity waveforms for high-power Naval Propulsion Drives (50-100 MW). This conclusion is based on the bulk inverter providing 100% of the real power while the hysteresis inverter acts as an active filter.

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APPENDIX A. MATLAB CODE AND SIMULINK SCHEMATICS

A. FILTER ANALYSIS M-FILE

```
% Generalized Impedance Converter
% by Brad Bittle
%07 September 2005
% Based on a circuit provided by Professor S. Michael

clc; clf; clear all;

%Initialization
syms s
s = tf('s');
R = 1000;  %R = 1000 ohms default
C = 1e-6;  %C = 1e-6 farads default
Q_p = 1/sqrt(2); %ideally flat case
f_g = 1e6;%GBWP in Hz (estimate for LM1458)
w_t = 2*pi*f_g;%same for both OpAmps
G = 1/R; %mhos
Y = (s*C);
B = G/Q_p;
w_o = 1/(R*C)
f_o = w_o/(2*pi)

%*******************************************************
%Filter     Y1  Y2  Y3      Y4  Y5  Y6  Y7  Y8  Transfer
%LP         G   Y   Y+B     G   G   0   0   G   T_2
%HP         G   G   Y       G   0   G   Y   B   T_1
%BP         G   G   Y       G   0   G   B   Y   T_1
%N          G   G   Y       G   G   0   Y   B   T_2
%AP         G   G   Y       G   G   0   Y   B   T_1
%*******************************************************
%Low Pass Filter
Y_1 = G;
Y_2 = Y;
Y_3 = Y+B;
Y_4 = G;
Y_5 = G;
Y_6 = 0;
Y_7 = 0;
Y_8 = G;

omega_n = sqrt(((Q_p + 1)/Q_p)*1/(R^2*C^2))
freq_n = omega_n/(2*pi)

%Ideal case (GBWP infinite)
num1 = (Y_1*Y_4*Y_5) + Y_3*Y_7*(Y_2 + Y_6) - (Y_3*Y_5*Y_8);
num2 = (Y_1*Y_4*Y_5) + (Y_2*Y_3*Y_7) + (Y_1*Y_5*Y_8) - (Y_1*Y_6*Y_7);
num3 = (Y_1*Y_4*Y_5) + (Y_2*Y_3*Y_7);
den = Y_1*Y_4*(Y_5 + Y_6) + Y_2*Y_3*(Y_7 + Y_8);

T_1 = num1/den;
T_2 = num2/den
T_3 = num3/den;
LPF = tf(T_2);%select desired transfer function (node dependent)
figure(1), hold on;
bode(LPF)
title('GIC Low Pass Filter Bode Plot')

poles = pole(LPF)
zeros = zero(LPF)
```

```
figure(2), hold on;
pzmap(LPF)

%nonideal case (GBWP 1 MHz)
a1 = ((Y_2 + Y_5 + Y_6)*(Y_1 + Y_3)*Y_7)/w_t;
a2 = ((Y_2 + Y_7 + Y_8)*(Y_1 + Y_3)*Y_5)/w_t;
b1 = (Y_1*Y_4*Y_5) + Y_3*Y_7*(Y_2 + Y_6) - (Y_3*Y_5*Y_8);
b2 = (Y_1*Y_4*Y_5) + (Y_2*Y_3*Y_7) + (Y_1*Y_5*Y_8) - (Y_1*Y_6*Y_7);
c = ((Y_4 + Y_7 + Y_8)*(Y_2 + Y_5 + Y_6) *(Y_1 +Y_3))/(w_t^2);
d = ((Y_4 + Y_7 + Y_8)*(Y_2 + Y_5 + Y_6) *(Y_1/w_t +Y_3/w_t));
e = Y_1*Y_4*(Y_5 + Y_6) + Y_2*Y_3*(Y_7 + Y_8);

T1_ni = (a1*s + b1)/(c*s^2 + d*s + e);
T2_ni = (a2*s + b2)/(c*s^2 + d*s + e);

sys_ni = tf(T2_ni);%select desired transfer function (node dependent)
%figure(1);
%bode(sys_ni)

poles_ni = pole(sys_ni)
zeros_ni = zero(sys_ni)
figure(2);
pzmap(sys_ni)

%All Pass Filter Transfer Function
R_1 = 9.25e3;
C_1 = 1e-6;
APF_num = s*R_1*C_1 -1;
APF_den = s*R_1*C_1 +1;
APF = APF_num/APF_den;

sys_APF = tf(APF)
figure(3), hold on;
bode(sys_APF)
title('All-Pass Filter Bode Plot')
APFpoles = pole(sys_APF)
APFzeros = zero(sys_APF)
figure(4)
pzmap(sys_APF)

Gain = -0.5;
Invert = -1;

F = Gain*Invert*T_2*APF;

sys_F = tf(F)
figure(5)
bode(sys_F)
title('Hysteresis Reference Signal Generation Filter')
Fpoles = pole(sys_F)
Fzeros = zero(sys_F)
figure(6)
pzmap(sys_F)

%end file
```

B. SIMULINK MODEL INITIALIZATION M.FILE:

```
% Bradford Bittle
% 22 August 2005
%Initialization m.file for SIMULINK hybrid parallelled inverter
%system model simulations

%***** clear MATLAB workspace, command line, and figures *****
clc;
clear all;
clf;

EN = 1; %enable double filtered reference feature

%***** start time, stop time *****
tstart = 0;%seconds
tstop = 0.25;%seconds

%***** DC Bus *****
Vdc = 100;              %dc bus voltage
                        %DC rails set at +0.5*Vdc and -0.5*Vdc

%***** Bulk Controller *****
f_c = 60;               %Hz (system frequency)
T_c = 1/f_c;            %period per cycle
omega_c = 2*pi*f_c;     %rad per sec

%***** Phase Delays for Pulses *****
%A = 0;                 %reference phase
B = (2/6)*T_c;
C = (4/6)*T_c;

%***** Hysteresis Tolerance bandwidth
%delta_h = 0.5;% 20% hysteresis band
%delta_h = 0.075;% 3% hysteresis band
delta_h = 0.05;% 2% hysteresis band

%***** Load resistance and inductance values *****

%***** coupling inductors *****
L_c = 2.5e-3; %mHenrys
R_c = 0.025; %Ohms (worst case assumed)

%***** RL load *****
L_l = 20e-3; %mHenrys
R_l = 10; %Ohms

%***** index for harmonics calculations *****
n = 21;

%***** Circuit leg impedance *****
R_t = R_c + R_l;
L_t = L_c + L_l;
X_t = zeros(n,1); %add 8 lines before printing for slide
Z = zeros(n,1);
Z_mag = zeros(n,1);
pF = zeros(n,1);
X_t(1) = 0;
Z(1) = R_t;
```

```
Z_mag(1) = abs(Z(1));
m = 6*n+1;
pF(1) = 0;
for k = 2:m
X_t(k) = (k-1)*omega_c*L_t;
pF(k) = X_t(k)/R_t;
Z(k) = R_t + j*X_t(k);
Z_mag(k) = abs(Z(k));
end
%end file
```

C. SIMULINK BLOCK SCHEMATICS

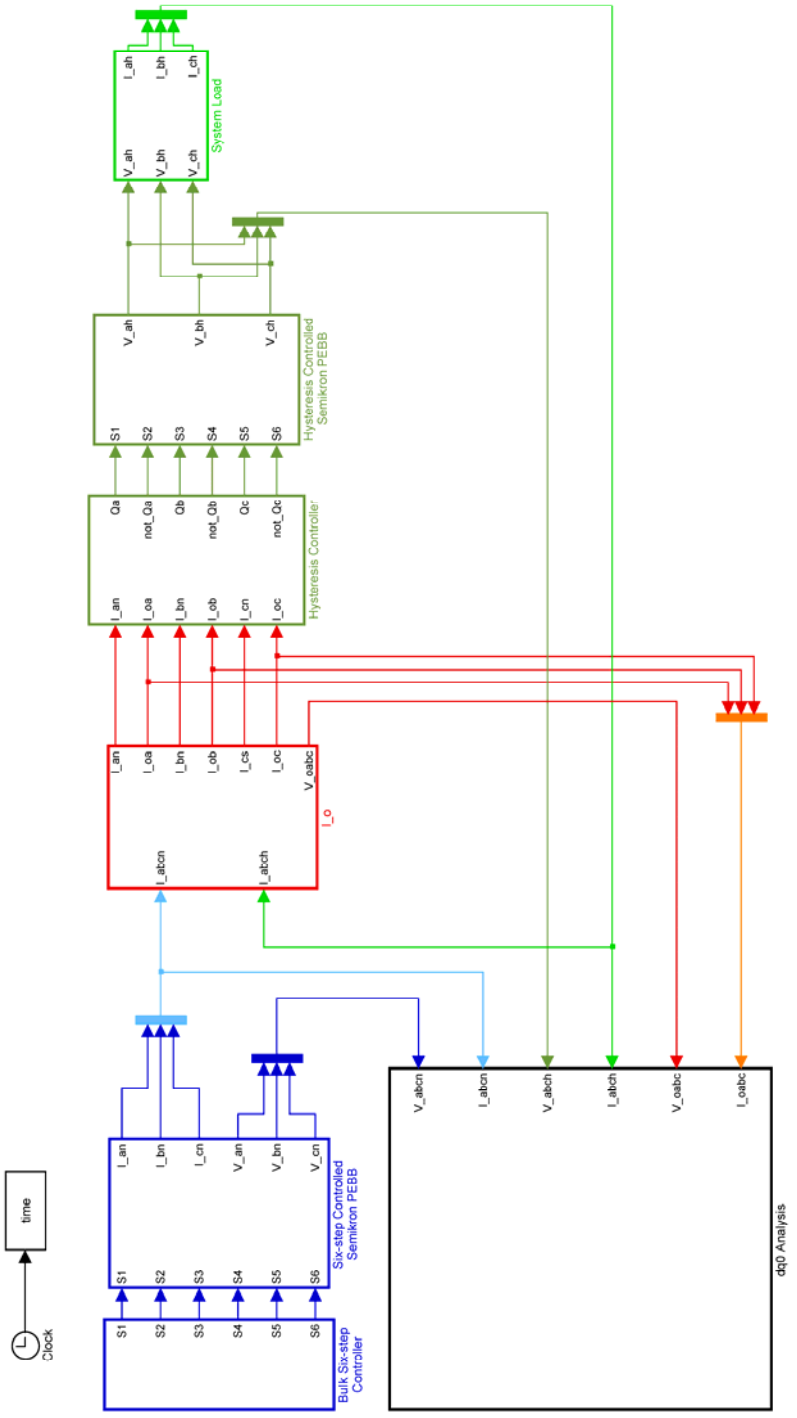


Figure 85. Three-phase PCHI SIMULINK Model

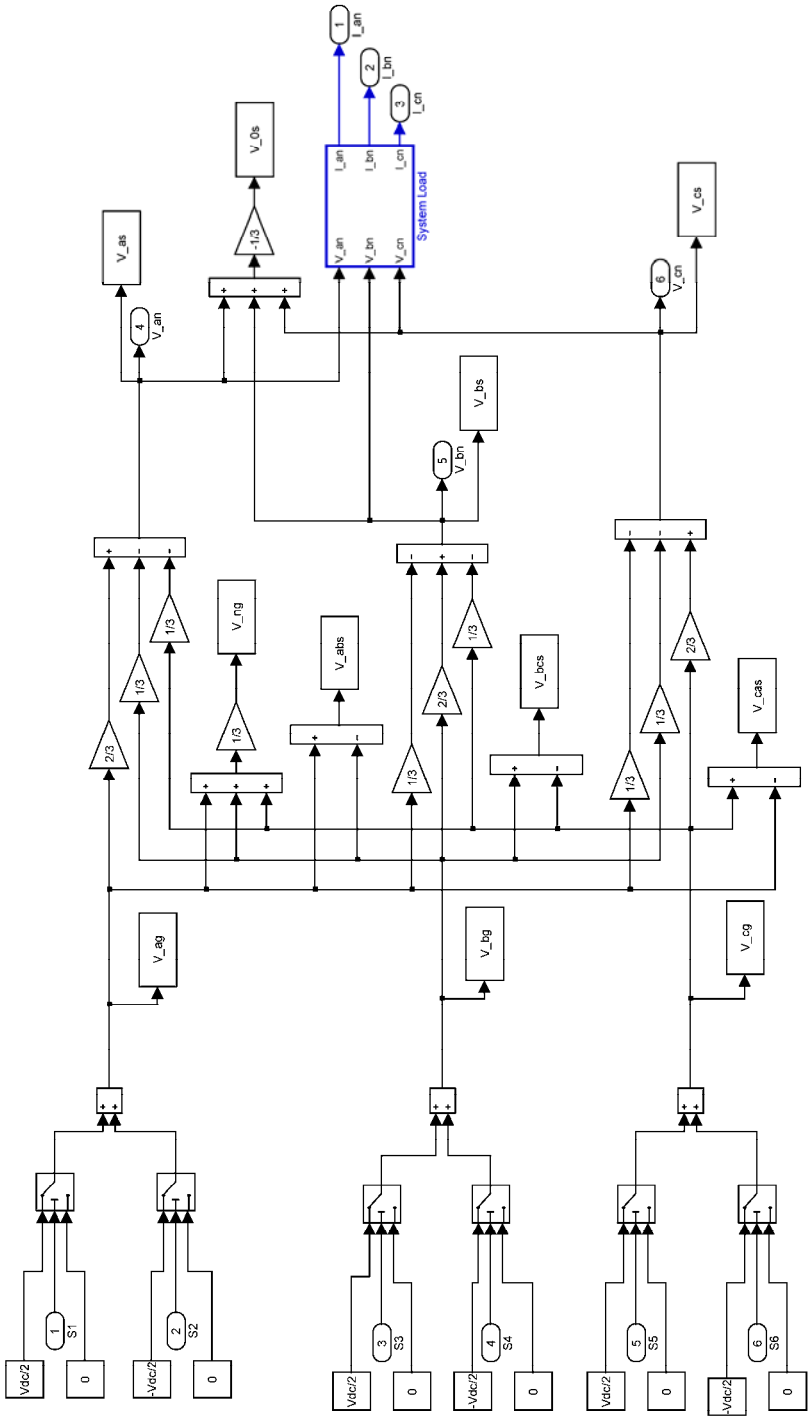


Figure 86. Three-phase Inverter Model (Bulk Inverter)

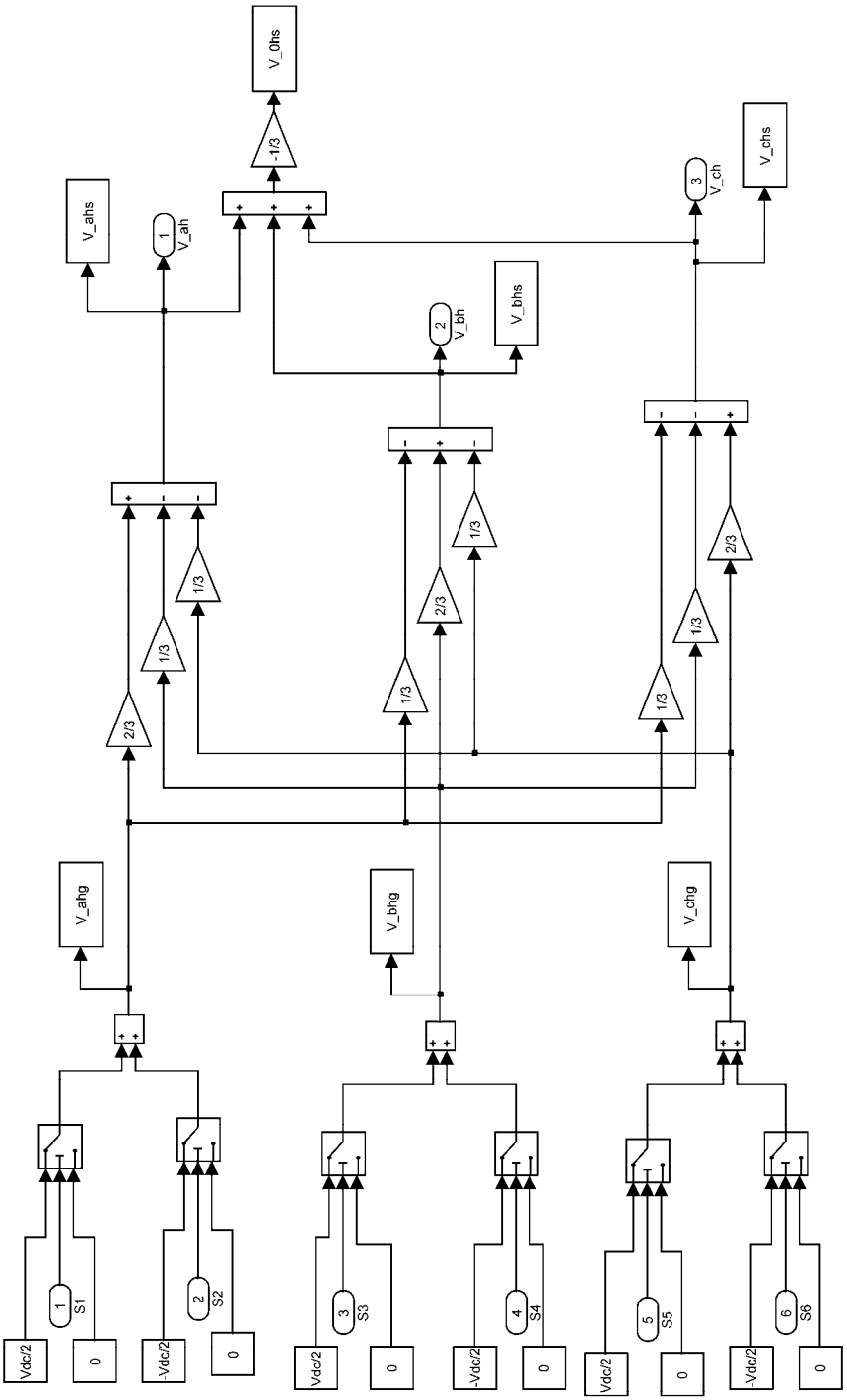


Figure 87. Three-phase Inverter Model (Hysteresis Inverter)

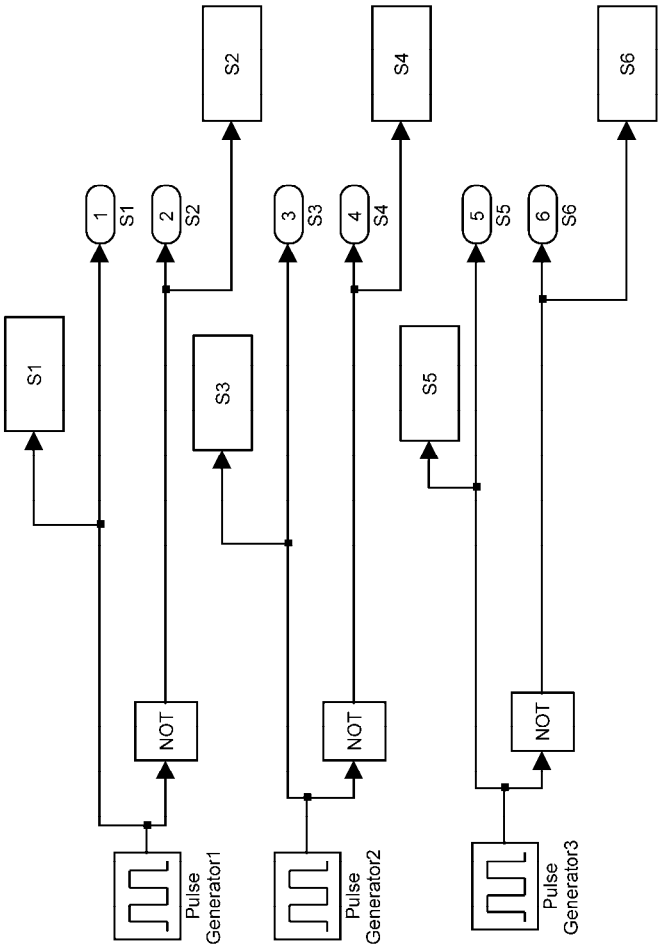


Figure 88. Bulk Six-Step Controller Model

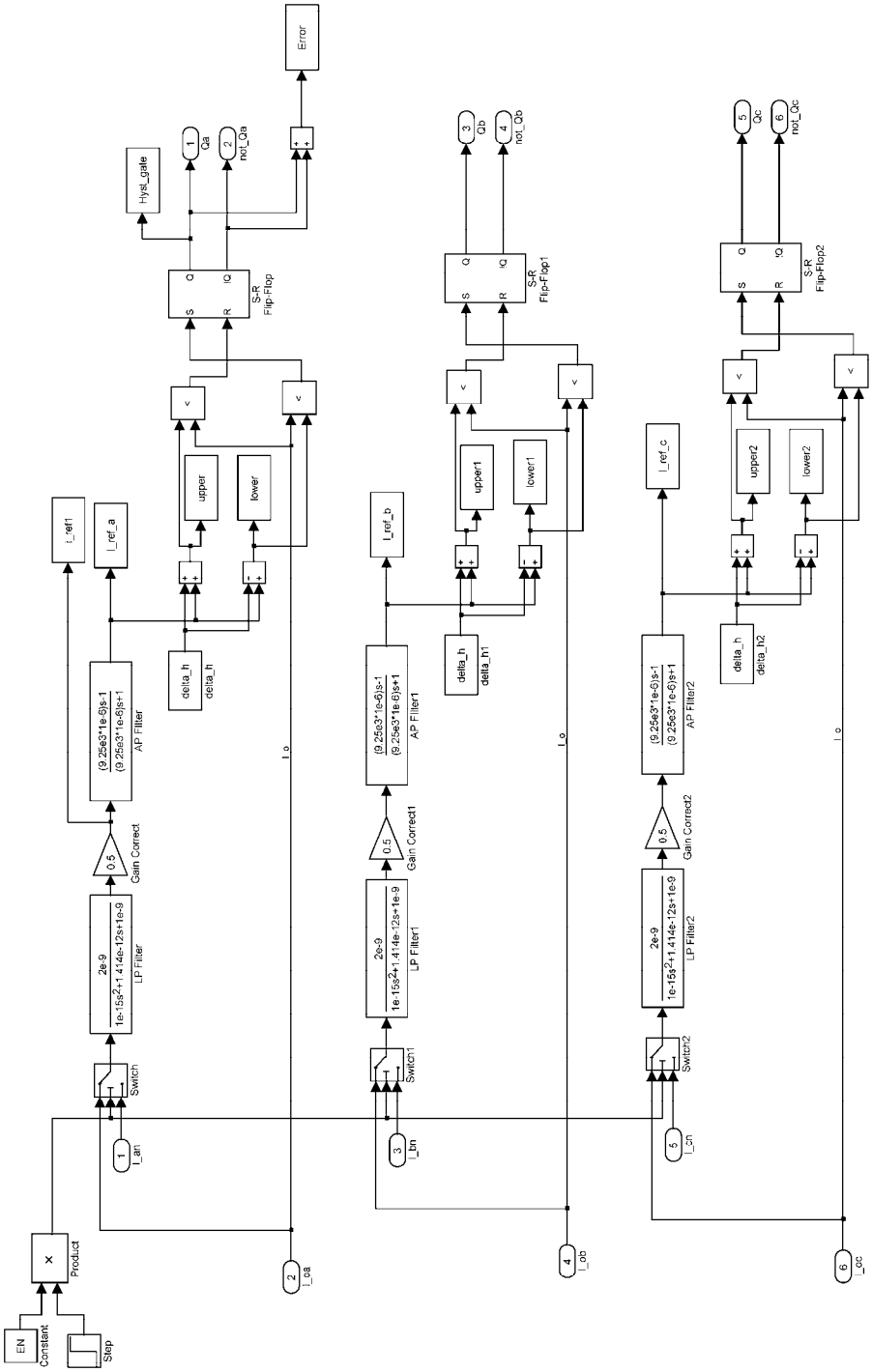
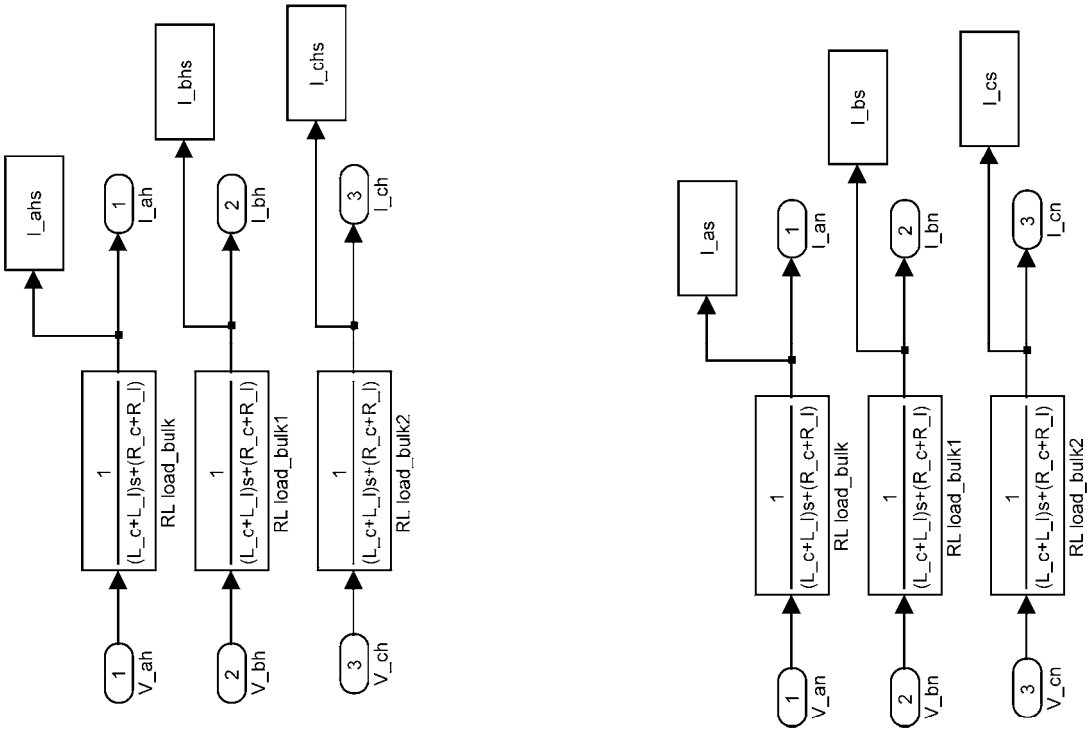


Figure 89. Hysteresis Controller Model



(a) (b)

Figure 90. Inverter Impedance Models (a) Hysteresis (b) Bulk

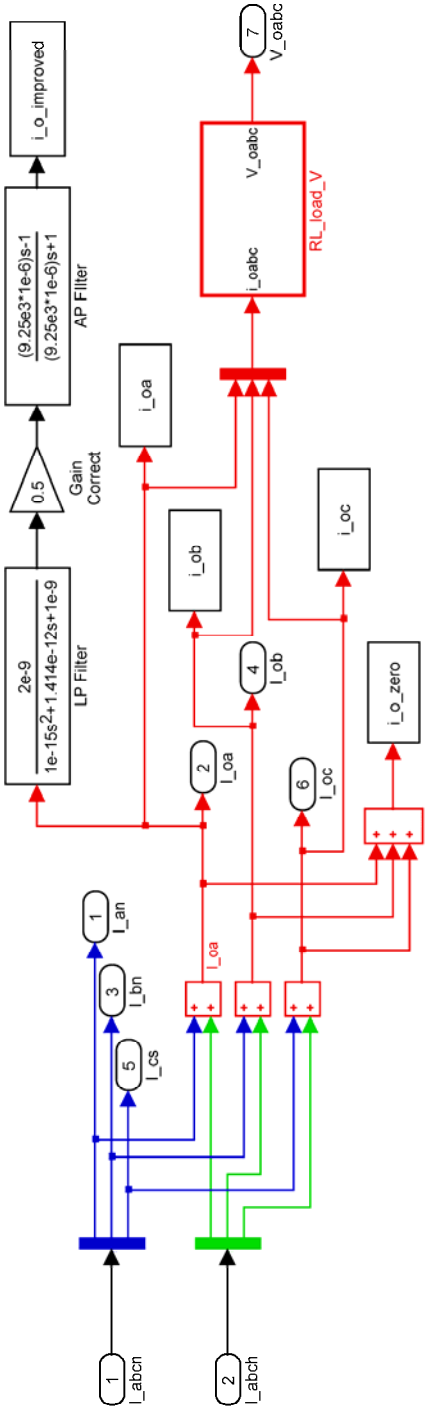


Figure 91. Load Current Calculations (with filtered reference analysis)

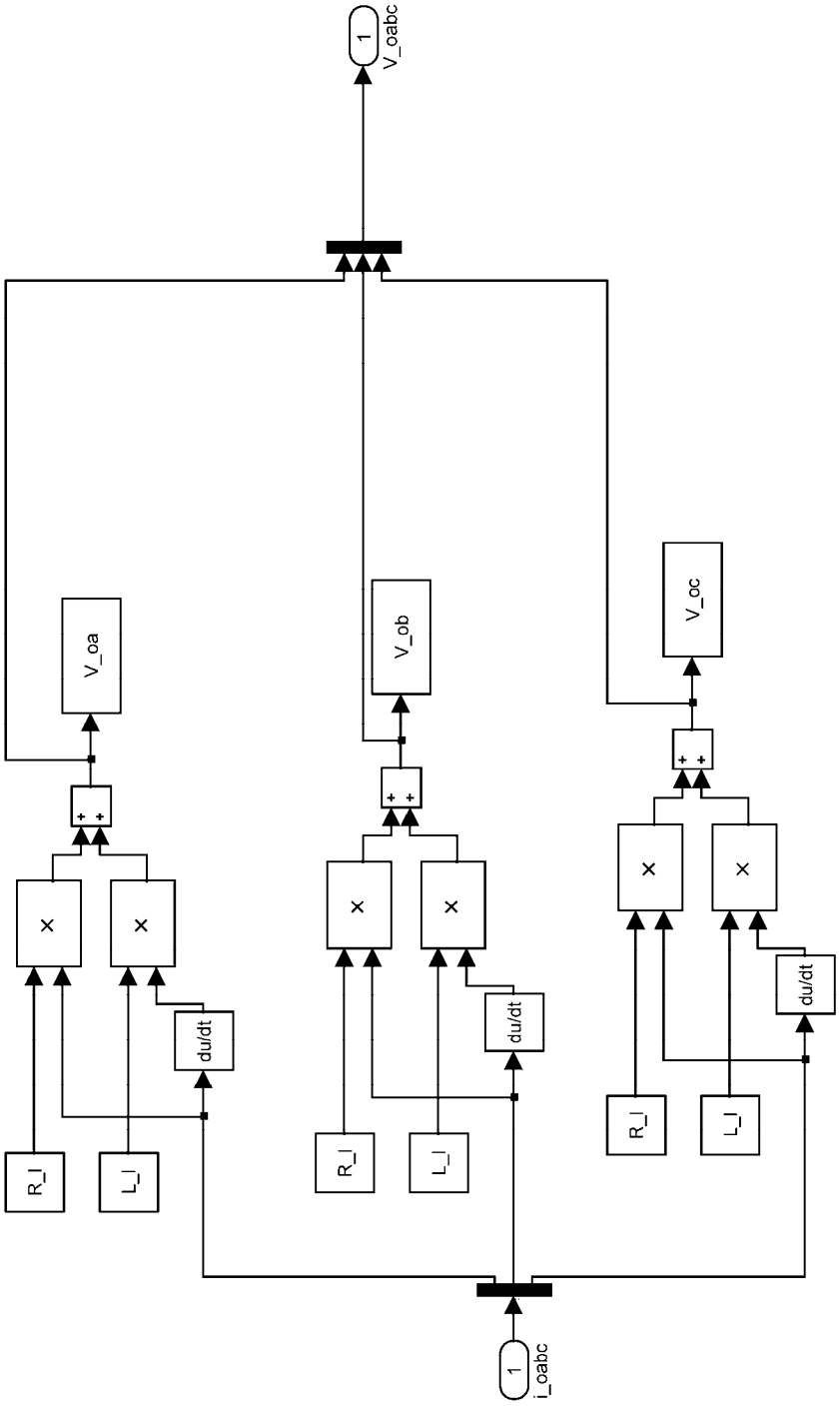


Figure 92. Load Voltage Waveform Calculations

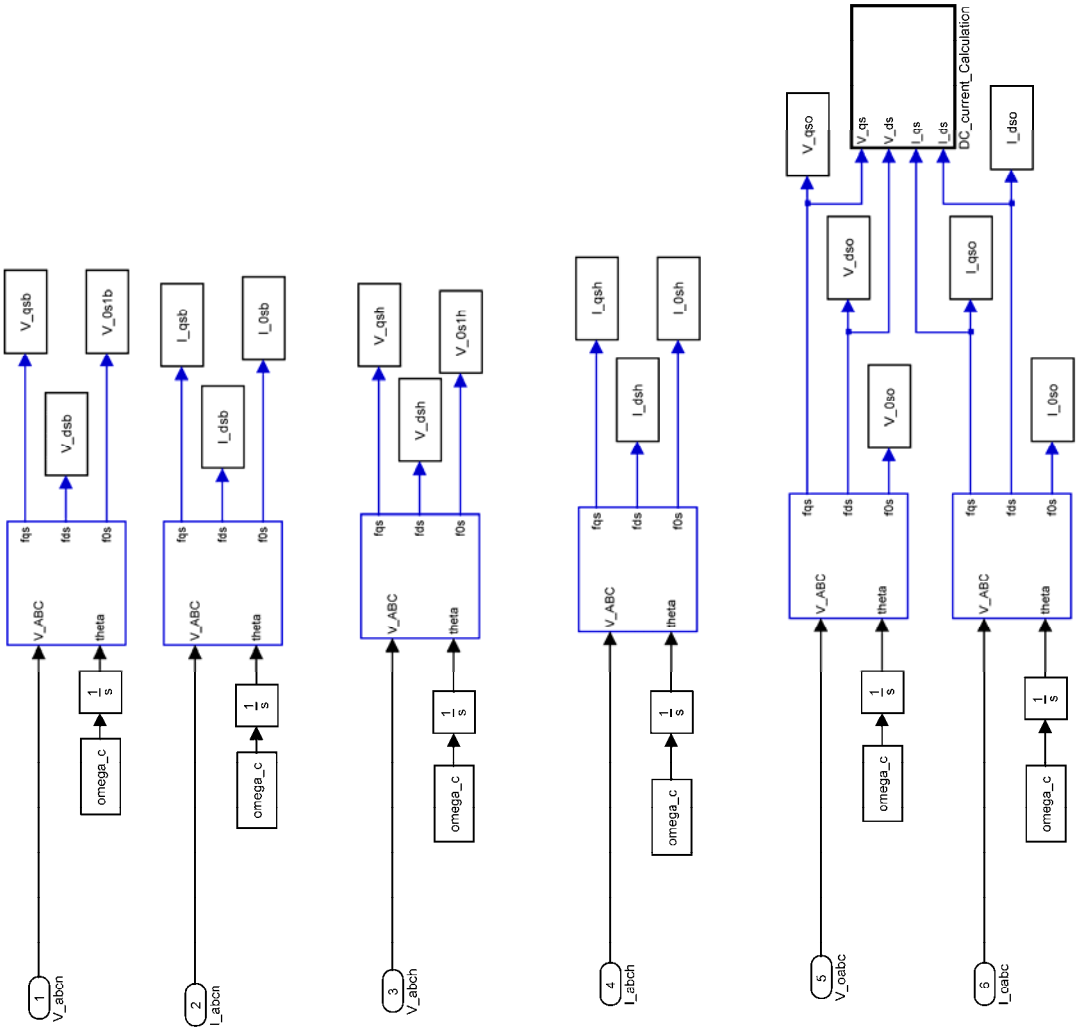


Figure 93. dq0 Reference Frame Module

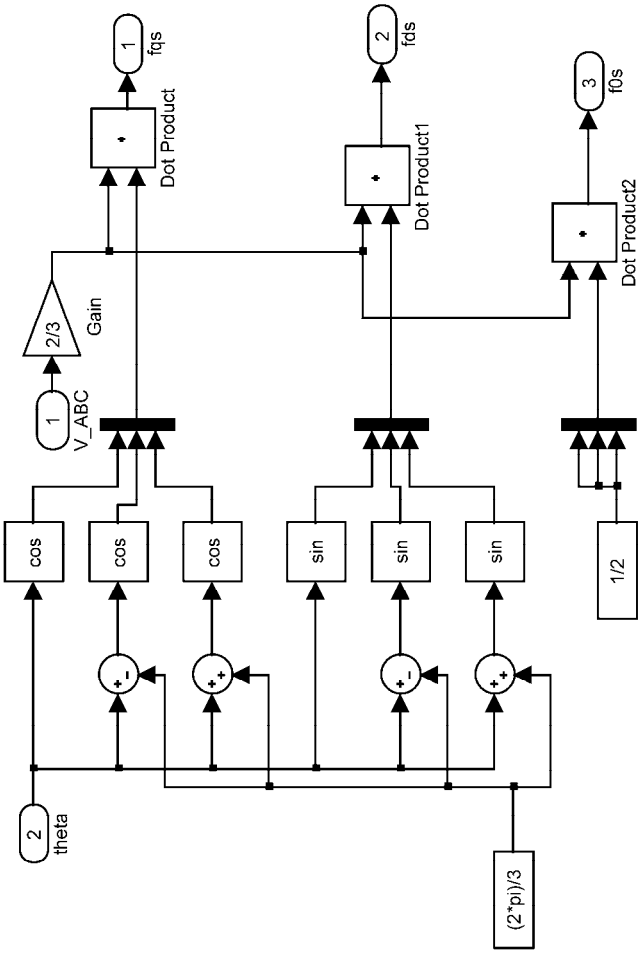


Figure 94. Parks Transform Calculation Module

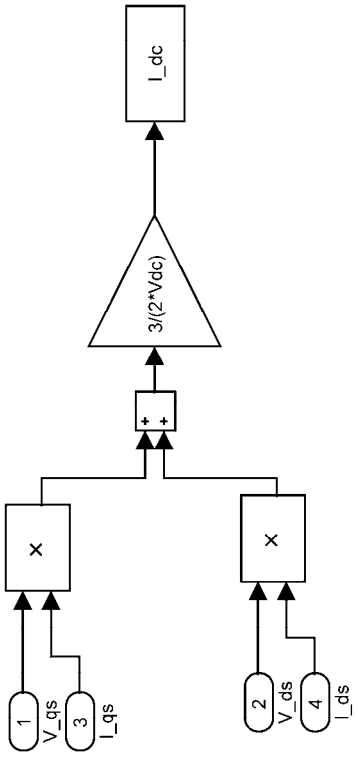


Figure 95. Input dc Current Calculation

D. OUTPUT ANALYSIS M-FILE

```
%Brad Bittle
%19 September 2005
%Three Phase Final Plots

%plot figs for data analysis
%   The subscripts for the variables extracted from the model
%are based on the equations given in Ref [12] and Ref [21].
%Plot subscripts are those used in the Thesis discussion.

clf;

%Bulk Inverter Component

%Bulk Controller Gate Trigger Signals
figure(1)
hold on
subplot(6,1,1)
plot(time(17866:23879), S1(17866:23879), 'b')
title('Bulk Gate Signals')
ylabel('S1')
subplot(6,1,2)
plot(time(17866:23879), S6(17866:23879), 'g')
ylabel('S6')
subplot(6,1,3)
plot(time(17866:23879), S3(17866:23879), 'r')
ylabel('S3')
subplot(6,1,4)
plot(time(17866:23879), S2(17866:23879), 'b')
ylabel('S2')
subplot(6,1,5)
plot(time(17866:23879), S5(17866:23879), 'g')
ylabel('S5')
subplot(6,1,6)
plot(time(17866:23879), S4(17866:23879), 'r')
ylabel('S4')
xlabel('time')

%Bulk Inverter Line-to-Neutral Voltages (All Phases)
figure(2)
hold on
subplot(3,1,1)
plot(time(17866:23879),V_as(17866:23879),'b')
grid on
ylabel('V_a_n (Volts)')
title('Line-to-Neutral Voltages')
subplot(3,1,2)
plot(time(17866:23879),V_bs(17866:23879),'r')
grid on
ylabel('V_b_n (Volts)')
subplot(3,1,3)
plot(time(17866:23879),V_cs(17866:23879),'g')
grid on
ylabel('V_c_n (Volts)')
xlabel('t(seconds')

%Bulk Inverter Line-to-Line Voltages
figure(3)
hold on
```

```
subplot(3,1,1)
plot(time(17866:23879),V_abs(17866:23879))
title('Line-to-Line Voltages')
ylabel('V_a_b (Volts)')
subplot(3,1,2)
plot(time(17866:23879),V_bcs(17866:23879))
ylabel('V_b_c (Volts)')
subplot(3,1,3)
plot(time(17866:23879),V_cas(17866:23879))
ylabel('V_c_a (Volts)')
xlabel('t(seconds)')

%Bulk Inverter Line-to-Neutral Current (Phase A)
figure(4)
plot(time(17866:23879),I_as(17866:23879))
grid on
title('Phase A Line-to-Neutral Current')
ylabel('I_a_n (Amps)')
xlabel('t(seconds)')

%Bulk Inverter Line-to-Neutral Voltage and Current Plot (Phase A)
figure(5)
hold on
subplot(2,1,1)
plot(time(17866:23879),V_as(17866:23879),'b')
grid on
title('Phase A Line-to-Neutral Voltage')
ylabel('V_a_n (Volts)')
subplot(2,1,2)
plot(time(17866:23879),I_as(17866:23879))
grid on
title('Phase A Line-to-Neutral Current')
ylabel('I_a_n (Amps)')
xlabel('t(seconds)')

%Bulk Inverter Neutral-to_Ground Voltage
figure(6)
plot(time(17866:23879),V_ng(17866:23879))
ylabel('V_n_g (Volts)')
title('Neutral-to-Ground Voltage')
xlabel('time (seconds)')

%Filter Analysis

%Filter Performance by Stages
figure(7)
hold on
%Input wave from Hall Effects
plot(time(17866:23879),I_as(17866:23879),'b')
%Low Pass Filter with Gain Correction
plot(time(17866:23879),i_ref1(17866:23879),'r')
%Phase Corrected
plot(time(17866:23879),I_ref_a(17866:23879),'g')
xlabel('t(seconds)')
ylabel('Amps')
title('Filter Waveform Comparison')

%Three Phase Reference Waveforms
```

```
figure(8)
hold on
plot(time(17866:23879),I_ref_a(17866:23879),'b')
plot(time(17866:23879),I_ref_b(17866:23879),'r')
plot(time(17866:23879),I_ref_c(17866:23879),'g')
xlabel('t(seconds)')
ylabel('Amps')
title('Phase Reference Waveform Comparison')

%Hysteresis Band Analysis
figure(9)
hold on

plot(time(17866:23879), upper(17866:23879), 'k', time(17866:23879), lower(17866:23879),'k'
, time(17866:23879), i_oa(17866:23879), 'b')
plot(time(17866:23879), upper1(17866:23879), 'k', time(17866:23879), lower1(17866:23879),
'k', time(17866:23879), i_ob(17866:23879), 'r')
plot(time(17866:23879), upper2(17866:23879), 'k', time(17866:23879), lower2(17866:23879),
'k', time(17866:23879), i_oc(17866:23879), 'g')
xlabel('t(seconds)')
ylabel('Amps')
title('Hysteresis Band Analysis')

%Double Filtered Reference Demonstration
figure(10)
hold on
subplot(2,1,1)
plot(time(17866:23879),I_as(17866:23879),'b',time(17866:23879),I_ref_a(17866:23879),'r')
title('Comparison between I_a_n and Filtered i_o_a')
subplot(2,1,2)
plot(time(17866:23879),i_oa(17866:23879),'b',time(17866:23879),i_o_improved(17866:23879),
'r')
xlabel('t(seconds)')
ylabel('Amps')
title('Comparison between i_o_a and Filtered i_o_a')

%Hysteresis Controled Inverter Voltage and Current Waveforms
figure(11)
hold on
subplot(2,1,1)
plot(time(17866:23879),V_ahs(17866:23879))
grid on;
ylabel('Volts')
title('Hysteresis Controller Voltage and Current Waveforms')
subplot(2,1,2)
plot(time(17866:23879),I_ahs(17866:23879))
grid on;
xlabel('t(seconds)')
ylabel('Amps')

%Bulk/Hysteresis Voltage and Current Comparison
figure(12)
hold on
subplot(4,1,1)
plot(time(17866:23879),V_as(17866:23879))
ylabel('Bulk Volts')
title('Voltage and Current Comparison')
subplot(4,1,2)
```

```
plot(time(17866:23879),I_as(17866:23879))
ylabel('Bulk Amps')
subplot(4,1,3)
plot(time(17866:23879),V_ahs(17866:23879))
ylabel('Hyst. Volts')
subplot(4,1,4)
plot(time(17866:23879),I_ahs(17866:23879))
ylabel('Hyst Amps')
xlabel('t(seconds)')

%Output Voltage and Current Waveforms
figure(13)
subplot(2,1,1)
plot(time(17866:23879),V_oa(17866:23879))
title('Load Voltage and Current Waveforms')
ylabel('Volts')
subplot(2,1,2)
plot(time(17866:23879),i_oa(17866:23879))
ylabel('Amps')
xlabel('t(seconds)')

% Quick Harmonic Check (Sum of Currents should equal zero)
figure(14)
plot(time(17866:23879),i_o_zero(17866:23879))
xlabel('t(seconds)')
ylabel('Amps')
title('Harmonic Content of i_o')

%DC Current Calculated
figure(15)
plot(time(17866:23879),I_dc(17866:23879))
title('DC Current Input')
ylabel('I_d_c (Amps)')
xlabel('time (seconds)')

I_dc_avg = mean(I_dc)

%THD Calcs
%Voltage Harmonics plot fourier series (abc reference frame)
Ah = zeros(n,1);
Bh = zeros(n,1);
h = zeros(n,1);
f = zeros(n,1);
Ah(1) = 0;
Ah(2) = (2/pi)*Vdc;
Bh(1) = 0;
Bh(2) = 0;
h(1) = 0;
h(2) = 1;
g(1) = 0;
f(1) = 0;
f(2) = 1;

for k = 1:n
    Ah(6*k-1) = (2/pi)*Vdc * (-1)^(k+1)/(6*k-1);
    Ah(6*k+1) = (2/pi)*Vdc * (-1)^k/(6*k+1);
    Bh(6*k-1) = -(2/pi)*Vdc * (-1)^(k+1)/(6*k-1);
    Bh(6*k+1) = -(2/pi)*Vdc * (-1)^k/(6*k+1);
```

```
    h(6*k-1) = abs(Ah(6*k-1)/Ah(2));
    h(6*k+1) = abs(Ah(6*k+1)/Ah(2));
    g(6*k-1) = abs(Bh(6*k-1)/Ah(2));
    g(6*k+1) = abs(Bh(6*k+1)/Ah(2));

end

m = 6*k+1;

for k = 2:m
    f(k) = k;
end

Ib = Ah./Z_mag;
Ih = Bh./Z_mag;
m = 6*n+1;

for k = 1:m
    b(k) = Ib(k)/Ib(2);
    h(k) = Ih(k)/Ib(2);
end

b = abs(b);
h = abs(h)';

%Plot of Bulk and Hysteresis Inverter Current Harmonics
figure(16)
hold on
subplot(2,1,1)
plot(f,b,'b')
title('Bulk Current Harmonic Content')
subplot(2,1,2)
plot(f,h,'r')
title('Hysteresis Current Harmonic Content')
xlabel('harmonic')

%Harmonic Cancellation Demonstration
figure(17)
plot(f,b-h,'b')
title('Harmonic Cancellation')
xlabel('harmonic')

Ib_squared = Ib.^2;
Ih_squared = Ih.^2;
ratio_bulk = zeros(n,1);
ratio_hyst = zeros(n,1);
sum_b = 0;
sum_h = 0;

for k = 3:n
    ratio_bulk = Ib_squared(k)/Ib_squared(2);
    ratio_hyst = Ih_squared(k)/Ib_squared(2);
    sum_b = sum_b + ratio_bulk;
    sum_h = sum_h + ratio_hyst;
end

THD_bulk = 100 * sqrt(sum_b)
THD_hyst = 100* sqrt(sum_h)
```

```
%instantaneous hysteresis switching frequency Try 2
Imax = max(I_ref_a(17866:23879));
Iref1 = abs(I_ref_a(17866:23879));
Iref1_squared = (Imax.^2-Iref1.^2);
xx = 4*(R_t)^2*Iref1_squared;
num1 = (Vdc^2-xx);
den1 = 4*L_t*(2*delta_h)*Vdc;

f_s1 = num1./den1;
f_s1_max = max(f_s1)
f_s1_min = min(f_s1)

figure(18)
hold on;
subplot(3,1,1)
plot(time(17866:23879), abs(I_ref_a(17866:23879)),'r')
title('Comparison of |I_r_e_f_a| versus switching frequency')
ylabel('|I_r_e_f_a (Amps)|')
subplot(3,1,2)
plot(time(17866:23879), Hyst_gate(17866:23879))
ylabel('Hys. Gate Signal (S1)')
subplot(3,1,3)
plot(time(17866:23879), f_s1,'k')
ylabel('frequency (Hz)')
xlabel('time (sec)')

%Hysteresis Controller Gate Trigger Signals
figure(19)
hold on
subplot(6,1,1)
plot(time(17866:23879), Hyst_gate(17866:23879), 'b')
title('Hysteresis Gate Control Signals')
axis([0.1, 0.13333, -0.1, 1.1])
ylabel('S1')
subplot(6,1,2)
plot(time(17866:23879), Hyst_gate6(17866:23879), 'g')
ylabel('S6')
axis([0.1, 0.13333, -0.1, 1.1])
subplot(6,1,3)
plot(time(17866:23879), Hyst_gate3(17866:23879), 'r')
ylabel('S3')
axis([0.1, 0.13333, -0.1, 1.1])
subplot(6,1,4)
plot(time(17866:23879), Hyst_gate2(17866:23879), 'b')
ylabel('S2')
axis([0.1, 0.13333, -0.1, 1.1])
subplot(6,1,5)
plot(time(17866:23879), Hyst_gate5(17866:23879), 'g')
ylabel('S5')
axis([0.1, 0.13333, -0.1, 1.1])
subplot(6,1,6)
plot(time(17866:23879), Hyst_gate4(17866:23879), 'r')
ylabel('S4')
axis([0.1, 0.13333, -0.1, 1.1])
xlabel('t(seconds)')

%end file
```

E. SIMULATION NOTES

To convert the controllers for discrete operation the following changes will be required:

The phase generators in the bulk controller will need to be replaced with a discrete source.

The filters used in the Hysteresis controller will need to be converted into the z-domain.

The load will need to be converted to a discrete form.

Other changes may be necessary to convert the continuous form of this model to discrete form to program it onto an FPGA.

APPENDIX B. CALCULATIONS

A. RELATIONSHIP BETWEEN THD AND DPF

377 rad/s		Z is unity	Vdc is 100V
R			
pF	X	L	THD
0.00001	0.0027	7.1618E-06	5.6681
0.0001	0.0027	7.1618E-06	5.6681
0.001	0.0027	7.1618E-06	5.6681
0.01	0.0027	7.1618E-06	5.6683
0.1	0.0026	6.8966E-06	5.6951
0.2	0.0026	6.8966E-06	5.7785
0.3	0.0025	6.6313E-06	5.926
0.4	0.0024	6.366E-06	6.1529
0.5	0.0023	6.1008E-06	6.487
0.6	0.0021	5.5703E-06	6.9803
0.7	0.0019	5.0398E-06	7.7399
0.8	0.0016	4.244E-06	9.0276
0.9	0.0012	3.183E-06	11.7469
0.99	0.000374	9.9204E-07	21.9313
0.999	0.000119	3.1565E-07	27.0897
0.9999	0.0000375	9.9469E-08	28.2662
1	0	0	28.4289

Table 16. THD vs. DPF Calculated Values

B. SINGLE PHASE HYSTERESIS SWITCHING FREQUENCY EQUATION DERIVATION

The equation used for the instantaneous switching frequency is:

$$f_s = \frac{V_{dc}^2 - 4R^2\left(I_{max}^2 - I_{refa}^2\right)}{8L_t\Delta_h V_{dc}} \tag{8.1}$$

The derivation of this equation follows:

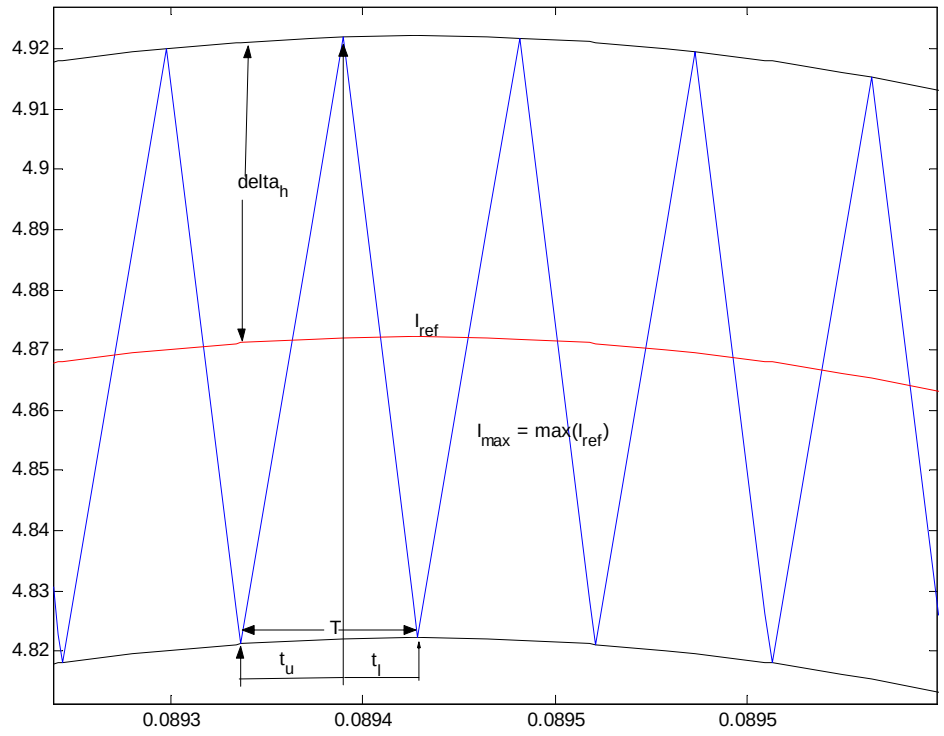


Figure 96. Hysteresis Band with Load Current

The switching period of one cycle is given as:

$$\frac{1}{f_s} = T_s. \tag{8.2}$$

The period consists of two distinct parts: the rise time and the fall time of the waveform (Fig. 96):

$$T_s = t_u + t_l \tag{8.3}$$

When the waveform is rising, the upper switch is closed and the current is pushed in the direction shown in Figure 97. When the waveform is falling, the lower switch is closed. The current still flows in the same direction as it cannot instantaneously change, but it begins to decrease in value as the potential across the resistance changes direction. The assumption that one and only one switch may be closed in a phase leg at any given moment holds.

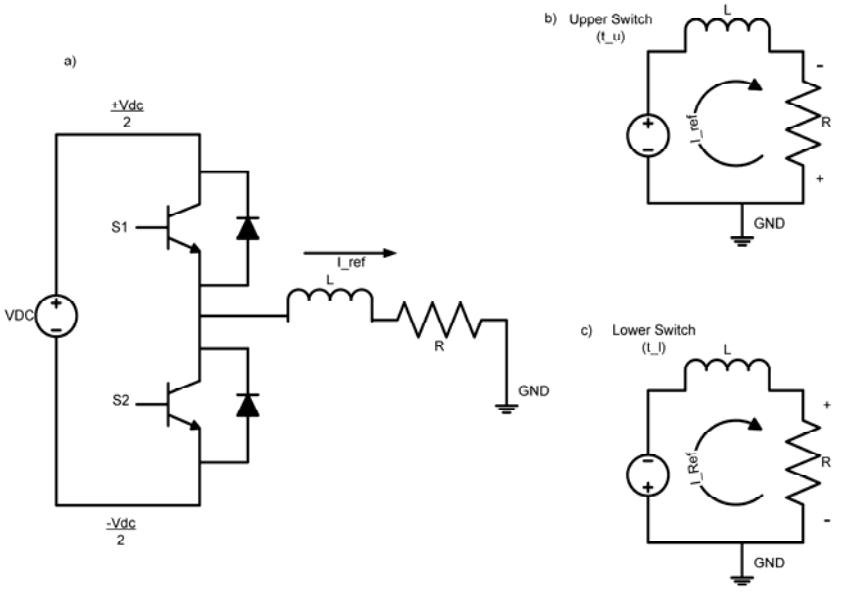


Figure 97. Representative System with Load

When the upper switch is closed, Ohm's law dictates:

$$L\frac{di}{dt} = \frac{V_{dc}}{2} + RI_{ref} \tag{8.4}$$

When the lower switch is closed:

$$\begin{aligned} -L\frac{di}{dt} &= \frac{-V_{dc}}{2} - RI_{ref} \text{ or,} \\ L\frac{di}{dt} &= \frac{V_{dc}}{2} + RI_{ref} \end{aligned} \tag{8.5}$$

If di is set to equal $2\Delta h$ and dt is set to equal the desired time interval (rise or fall time) then the following relationships can be obtained:

$$\begin{aligned} \text{Rise time: } \frac{2L\Delta h}{t_u} &= \frac{V_{dc}}{2} - RI_{ref} \\ \text{Fall time: } \frac{2L\Delta h}{t_l} &= \frac{V_{dc}}{2} + RI_{ref} \end{aligned} \tag{8.6}$$

Using these relationships the rise and fall times can be calculated:

$$\begin{aligned} \frac{1}{t_u} &= \frac{1}{2L\Delta h}\left[\frac{V_{dc}}{2} - RI_{ref}\right] = \frac{V_{dc} - 2RI_{ref}}{4L\Delta h} \\ \frac{1}{t_l} &= \frac{1}{2L\Delta h}\left[\frac{V_{dc}}{2} + RI_{ref}\right] = \frac{V_{dc} + 2RI_{ref}}{4L\Delta h} \\ t_u &= \frac{4L\Delta h}{V_{dc} - 2RI_{ref}} \\ t_l &= \frac{4L\Delta h}{V_{dc} + 2RI_{ref}} \end{aligned} \tag{8.7}$$

Using equation 8.3 to get the entire period:

$$\begin{aligned} T_s &= \frac{4L\Delta h}{V_{dc} - 2RI_{ref}} + \frac{4L\Delta h}{V_{dc} + 2RI_{ref}} \\ T_s &= \frac{4L\Delta h\left(V_{dc} + 2RI_{ref}\right) + 4L\Delta h\left(V_{dc} - 2RI_{ref}\right)}{\left(V_{dc} - 2RI_{ref}\right)\left(V_{dc} + 2RI_{ref}\right)} \\ T_s &= \frac{4L\Delta h\left(V_{dc} + 2RI_{ref}\right) + 4L\Delta h\left(V_{dc} - 2RI_{ref}\right)}{\left(V_{dc} - 2RI_{ref}\right)\left(V_{dc} + 2RI_{ref}\right)} \\ T_s &= \frac{8L\Delta h V_{dc}}{V_{dc}^2 - \left(2RI_{ref}\right)^2} \end{aligned} \tag{8.8}$$

The instantaneous switching frequency is therefore:

$$f_s = \frac{V_{dc}^2 - \left(2RI_{ref}\right)^2}{8L\Delta h V_{dc}} \tag{8.9}$$

This result is contrary to the experimental results obtained in References 9 and 10 in that the maximum switching frequency occurs at the zero crossing. To shift the frequency so that the fastest switching rates occur at the maxima and minima values of

the reference the current is scaled by the maximum value of the reference. Thus the final formula:

$$f_s = \frac{V_{dc}^2 - 4R^2\left(I_{max}^2 - I_{refa}^2\right)}{8L_t\Delta_h V_{dc}} \tag{8.10}$$

The frequency now matches the observational data (Fig. 98).

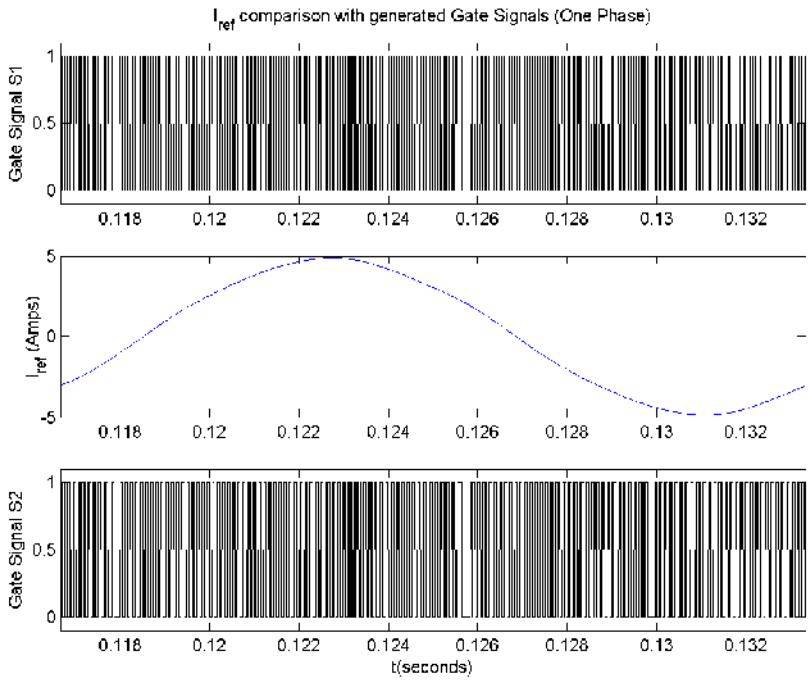


Figure 98. Single Phase Comparison Hysteresis Gate Signal versus the Reference Waveform

C. GIC FILTER NON-IDEAL TRANSFER FUNCTION DERIVATION

Assuming non-ideal Op-amp find the transfer functions for T_1 and T_2 (given in Chapter III);

Node equations $\left(\omega_t = 1*10^{-6}\right)$:

$$V_1=A_2(V_3 - V_4);\ A_2 = \frac{\omega_{t_2}}{s} \tag{8.11}$$

$$V_2=A_1(V_5 - V_4);\ A_1 = \frac{\omega_{t_1}}{s} \tag{8.12}$$

$$V_2Y_4+V_IY_7 = V_3(Y_4+Y_7+Y_8);\ \text{Let } w = (Y_4+Y_7+Y_8)$$
$$V_3 = \frac{(V_2Y_4 + V_IY_7)}{w} \tag{8.13}$$

$$V_4(Y_1+Y_3) = V_2Y_3+V_1Y_1;\qquad \text{Let } z = (Y_1+Y_3)$$
$$V_4 = \frac{(V_2Y_3 + V_1Y_1)}{z} \tag{8.14}$$

$$V_1Y_2+V_IY_5 = V_5(Y_2+Y_5+Y_6);\quad \text{Let } x = (Y_2+Y_5+Y_6)$$
$$V_5 = \frac{(V_1Y_2 + V_IY_5)}{x} \tag{8.15}$$

Substitute (8.13) and (8.14) into (8.11):

$$V_1 = A_2\left[\frac{(V_2Y_4 + V_IY_7)}{w} - \frac{(V_2Y_3 + V_1Y_1)}{z}\right] \tag{8.16}$$
$$V_1(wz + A_2wY_1) = V_2(A_2zY_4 - A_2wY_3) + V_I(A_2zY_7)$$

$$V_1 = V_2\left(\frac{A_2zY_4 - A_2wY_3}{wz + A_2wY_1}\right) + V_I\left(\frac{A_2zY_7}{wz + A_2wY_1}\right) \tag{8.17}$$

Substitute (8.14) and (8.15) into (8.12):

$$V_2=A_1\left[\frac{(V_1Y_2 + V_IY_5)}{x} - \frac{(V_2Y_3 + V_1Y_1)}{z}\right] \tag{8.18}$$
$$V_2(xz+A_2xY_3) = V_1(A_1zY_2 - A_1xY_1) + V_I(A_1zY_5)$$

$$V_2 = V_1\left(\frac{A_1zY_2 - A_1xY_1}{xz + A_1xY_3}\right) + V_I\left(\frac{A_1zY_5}{xz + A_1xY_3}\right) \tag{8.19}$$

To find $\frac{V_1}{V_I}$, substitute (8.19) into (8.17):

$$V_1 = \left[V_1\left(\frac{A_1zY_2 - A_1xY_1}{xz + A_1xY_3}\right) + V_I\left(\frac{A_1zY_5}{xz + A_1xY_3}\right)\right]\left(\frac{A_2zY_4 - A_2wY_3}{wz + A_2wY_1}\right) + V_I\left(\frac{A_2zY_7}{wz + A_2wY_1}\right) \tag{8.20}$$

After much algebraic manipulation:

$$\begin{aligned}
T_1 &= \frac{V_1}{V_I} = \left\{\frac{As + B}{Cs^2 + Ds + E}\right\} \\
A &= \left[\frac{(Y_2 + Y_5 + Y_6)(Y_1 + Y_3)Y_7}{\omega_{t_1}}\right] \\
B &= \left(Y_1Y_4Y_5 + Y_2Y_3Y_7 + Y_3Y_6Y_7 - Y_3Y_5Y_8\right) \\
C &= \left[\frac{\left(Y_4 + Y_7 + Y_8\right)\left(Y_2 + Y_5 + Y_6\right)(Y_1 + Y_3)}{\omega_{t_1}\omega_{t_2}}\right] \\
D &= \left[\left(Y_4 + Y_7 + Y_8\right)\left(Y_2 + Y_5 + Y_6\right)\left(\frac{Y_3}{\omega_{t_2}} + \frac{Y_1}{\omega_{t_1}}\right)\right] \\
E &= \left[Y_2Y_3(Y_7 + Y_8) + Y_1Y_4(Y_5 + Y_6)\right]
\end{aligned} \tag{8.21}$$

To find $\frac{V_2}{V_I}$, substitute (8.17) into (8.19):

$$V_2 = \left[V_2\left(\frac{A_2zY_4 - A_2wY_3}{wz + A_2wY_1}\right) + V_I\left(\frac{A_2zY_7}{wz + A_2wY_1}\right)\right]\left(\frac{A_1zY_2 - A_1xY_1}{xz + A_1xY_3}\right) + V_I\left(\frac{A_1zY_5}{xz + A_1xY_3}\right) \tag{8.22}$$

After much algebraic manipulation:

$$
\begin{aligned}
T_2 &= \frac{V_2}{V_I} = \left\{ \frac{As + B}{Cs^2 + Ds + E} \right\} \\
A &= \left[\frac{(Y_2 + Y_7 + Y_8)(Y_1 + Y_3) Y_5}{\omega_{t_2}} \right] \\
B &= \left(Y_2 Y_3 Y_7 + Y_1 Y_5 Y_4 + Y_1 Y_5 Y_8 - Y_1 Y_6 Y_7 \right) \\
C &= \left[\frac{(Y_4 + Y_7 + Y_8)(Y_2 + Y_5 + Y_6)(Y_1 + Y_3)}{\omega_{t_1} \omega_{t_2}} \right] \\
D &= \left[(Y_4 + Y_7 + Y_8)(Y_2 + Y_5 + Y_6) \left(\frac{Y_3}{\omega_{t_2}} + \frac{Y_1}{\omega_{t_1}} \right) \right] \\
E &= \left[Y_2 Y_3 (Y_7 + Y_8) + Y_1 Y_4 (Y_5 + Y_6) \right]
\end{aligned}
\tag{8.23}
$$

D. ALL-PASS FILTER CALCULATIONS

Lead Configuration Desired:

$$
\begin{aligned}
&\theta(\omega) = 32^\circ \\
&32 = 180 - 2\tan^{-1}(\omega RC) \\
&\text{Let } C = 1\mu F \text{ and } \omega = 377 \text{ rad/s} \\
&148 = 2\tan^{-1}(\omega RC) \\
&74 = \tan^{-1}(\omega RC) \\
&R = \frac{\tan(74)}{377 \text{rad/s} \cdot 10^{-6} \text{F}} = 9.25\ \text{k}\Omega \\
&9.25\ \text{k}\Omega = 9.1\text{k}\Omega + 150\text{k}\Omega
\end{aligned}
\tag{8.24}
$$

The actual phase-shift observed with the GIC LPF is -31.9°. The resistance required is therefore 9.281Ω.

APPENDIX C. CIRCUIT BOARD LAYOUTS AND PARTSLISTS

A. BULK SIX-STEP CONTROLLER

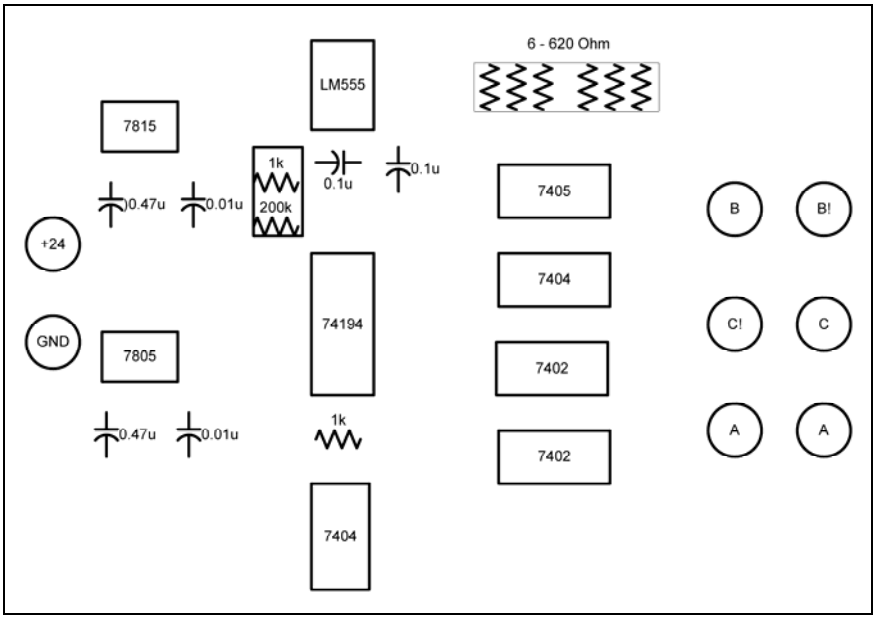


Figure 99. Bulk Six-Step Controller Board Map

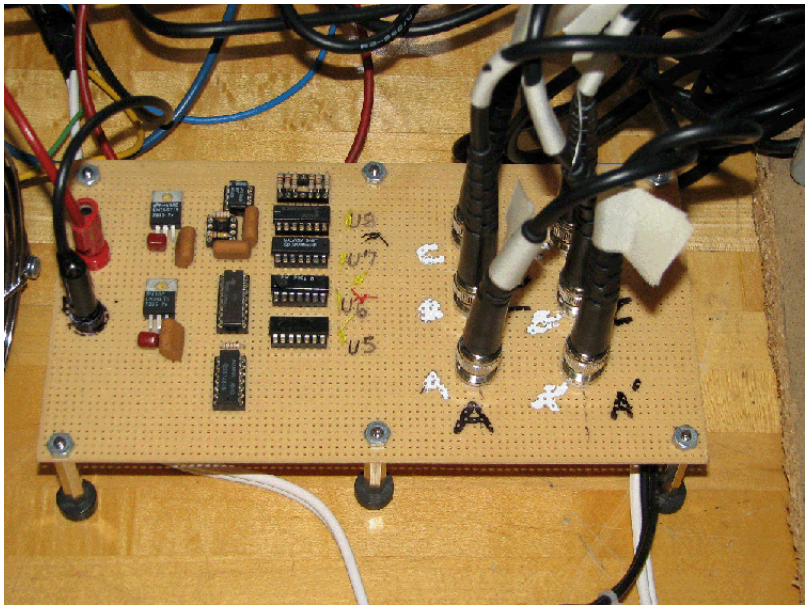


Figure 100. Bulk Controller

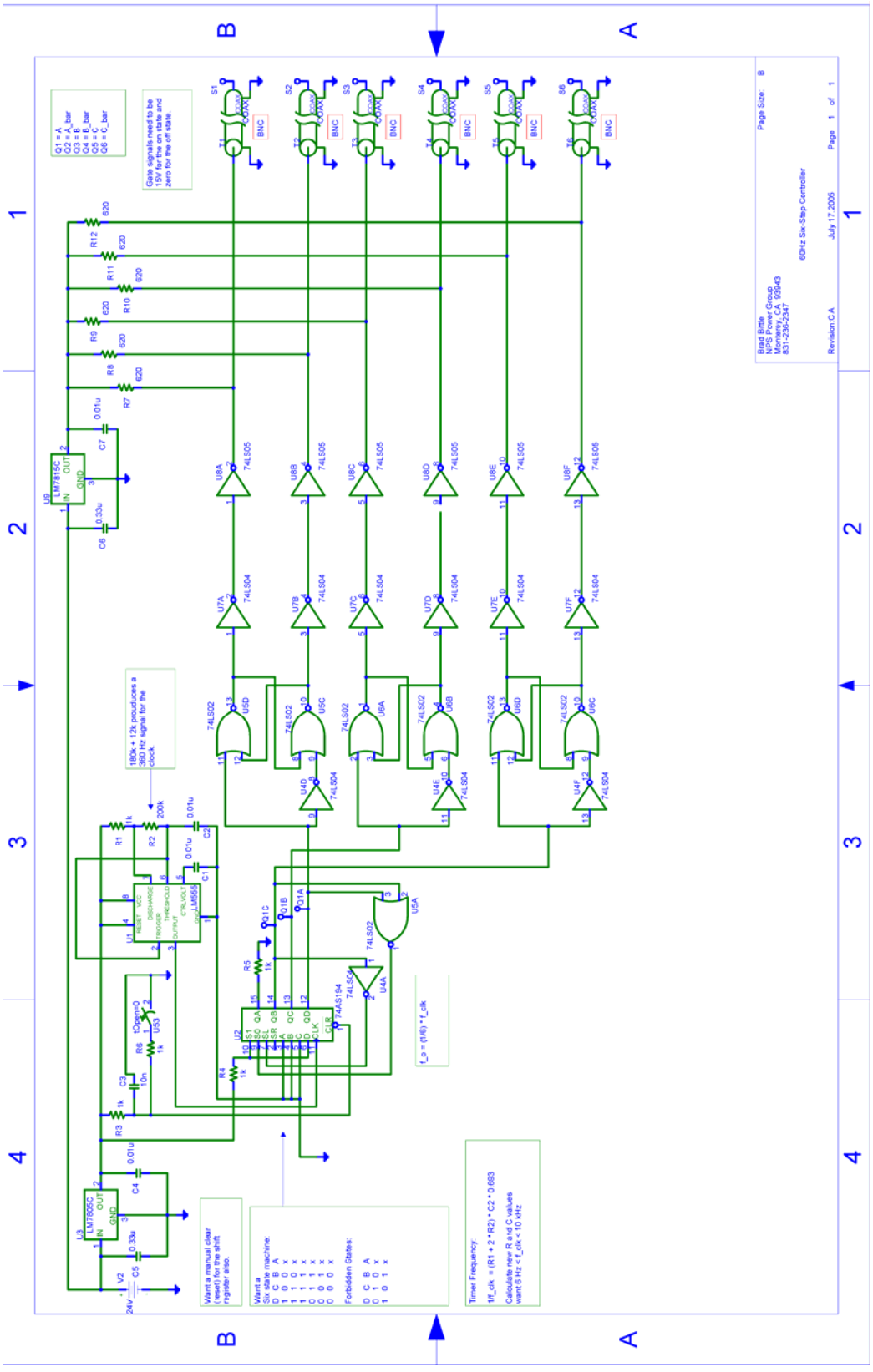


Figure 101. Bulk Controller Schematic

B. HYSTERESIS CONTROLLER HALL EFFECT SENSORS

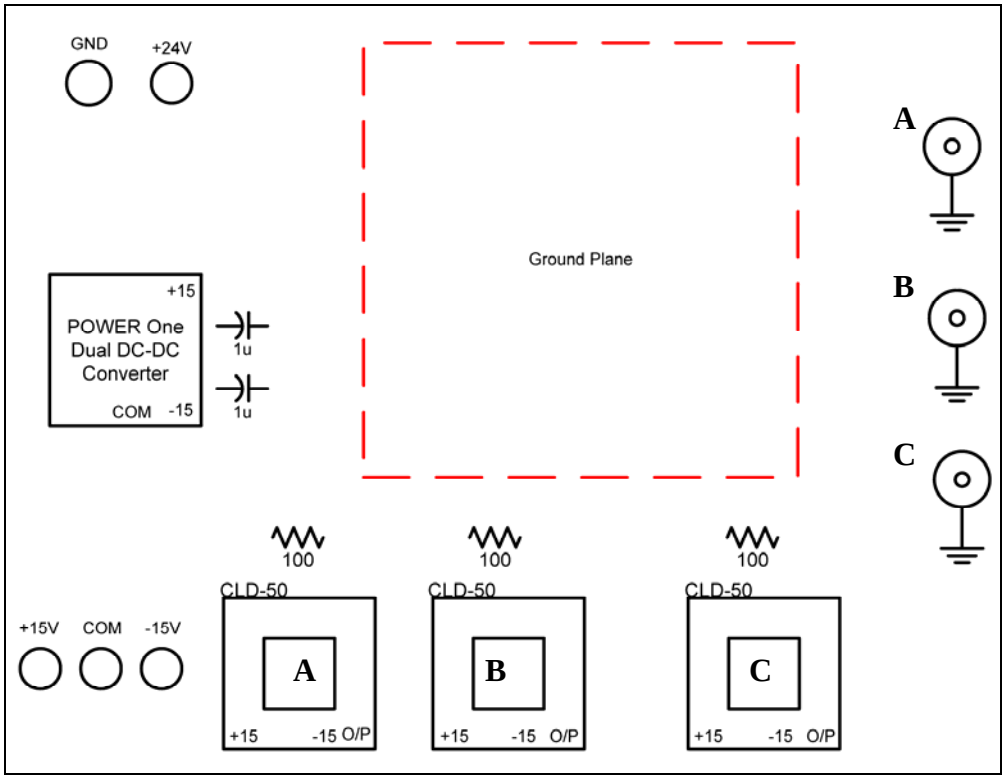


Figure 102. Hall Effect Sensor Board Map

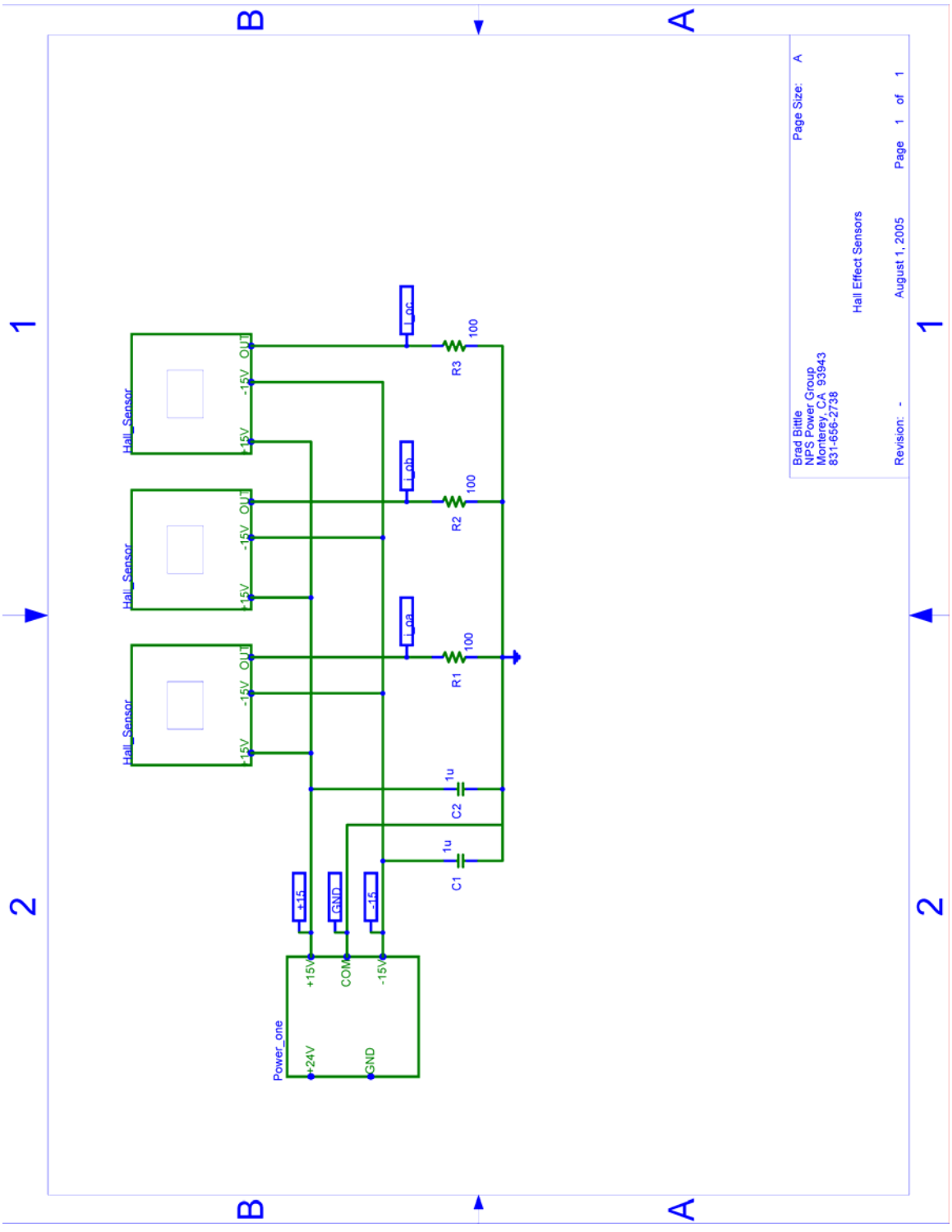


Figure 103. Hall Effect Circuit Schematic

C. HYSTERESIS CONTROLLER – FILTER CIRCUIT

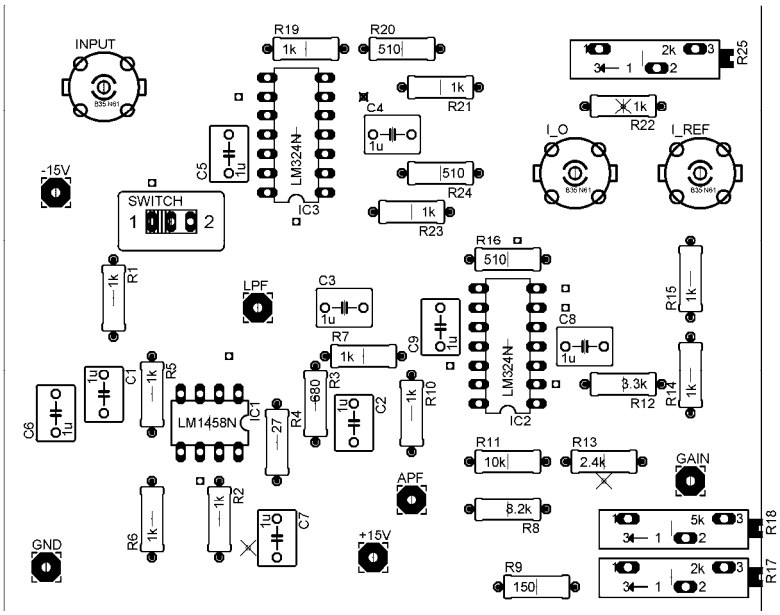


Figure 104. Filter Circuit Board Map (One Phase only)

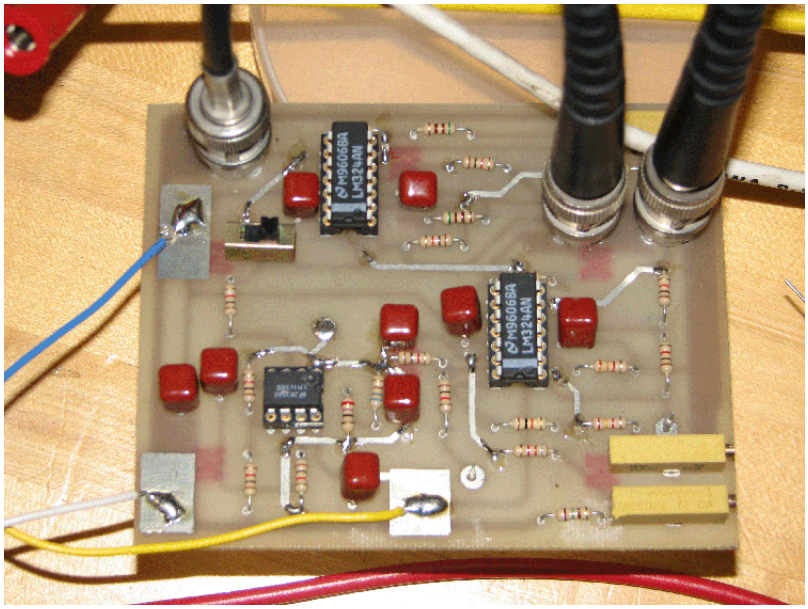


Figure 105. Filter Circuit Board (One Phase only)

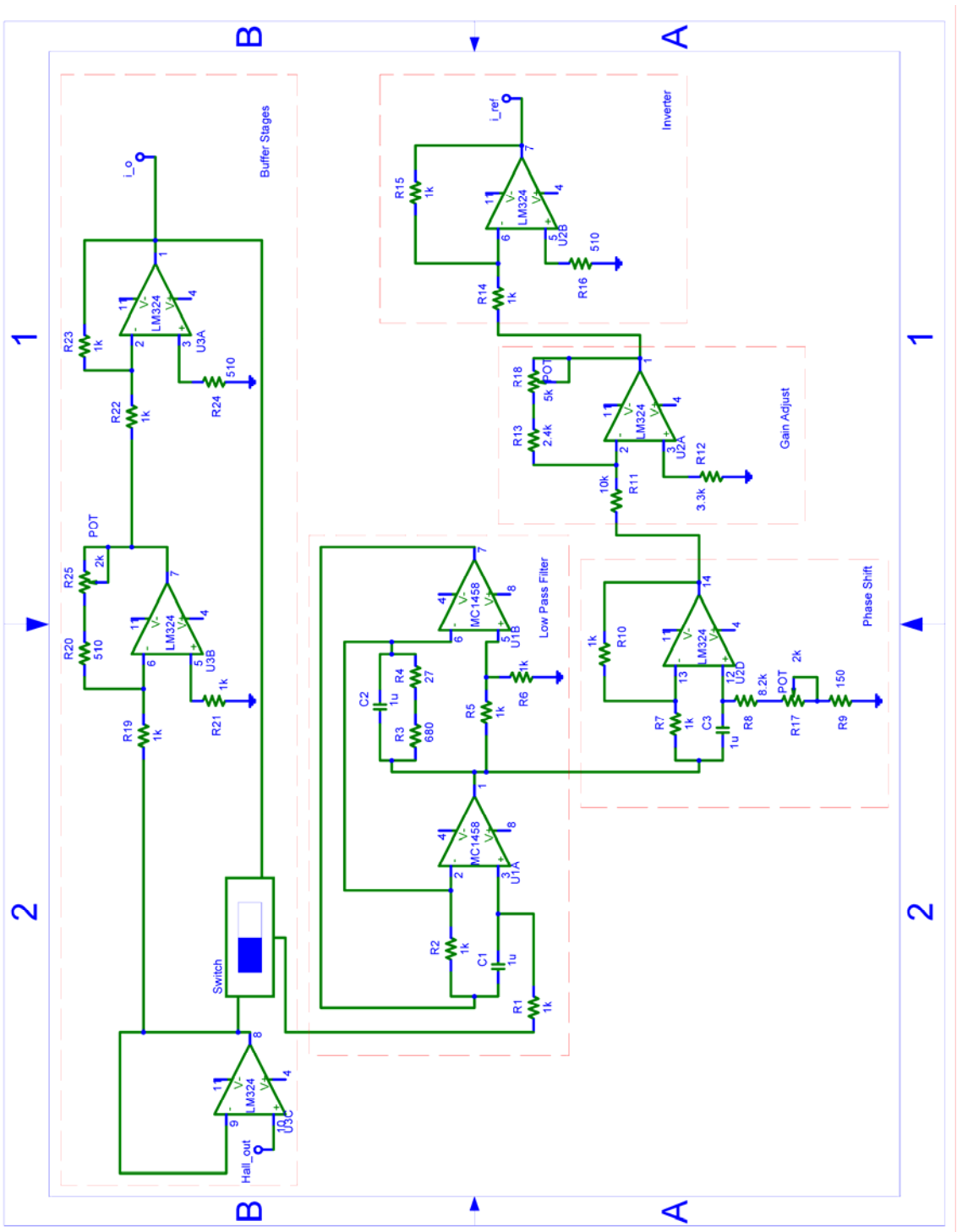


Figure 106. Hysteresis Filter Circuit Schematic (One Phase Only)

D. HYSTERESIS CONTROLLER – HYSTERESIS CIRCUIT

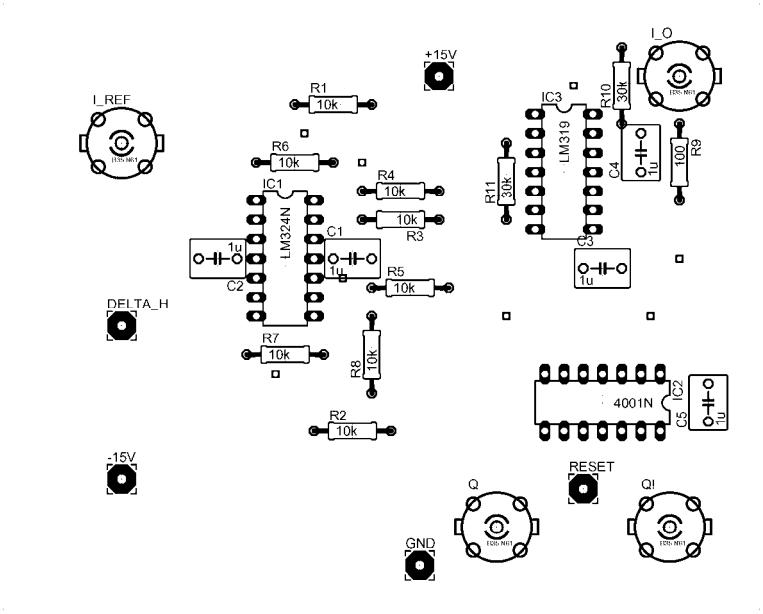


Figure 107. Hysteresis Circuit Board Layout (One Phase only) [Not used this thesis effort]

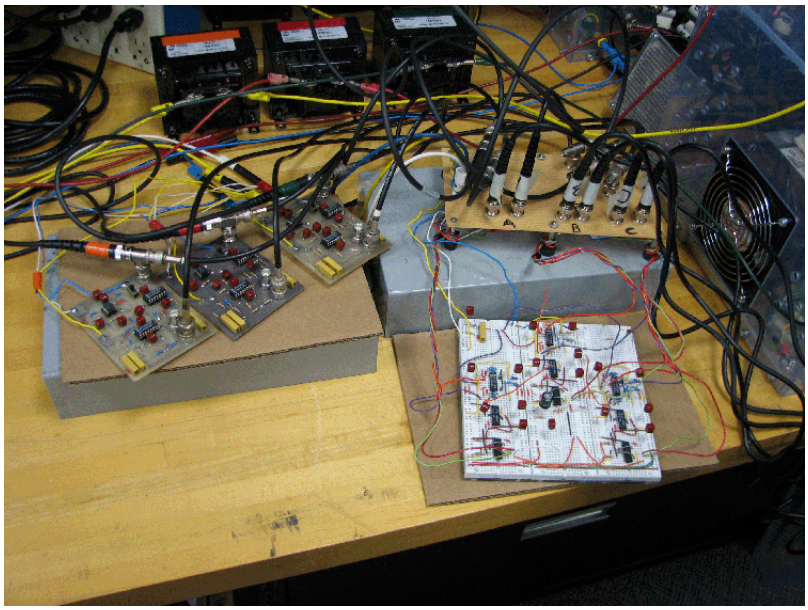


Figure 108. Hysteresis Controller Filter, Patch Panel and Hysteresis Circuit

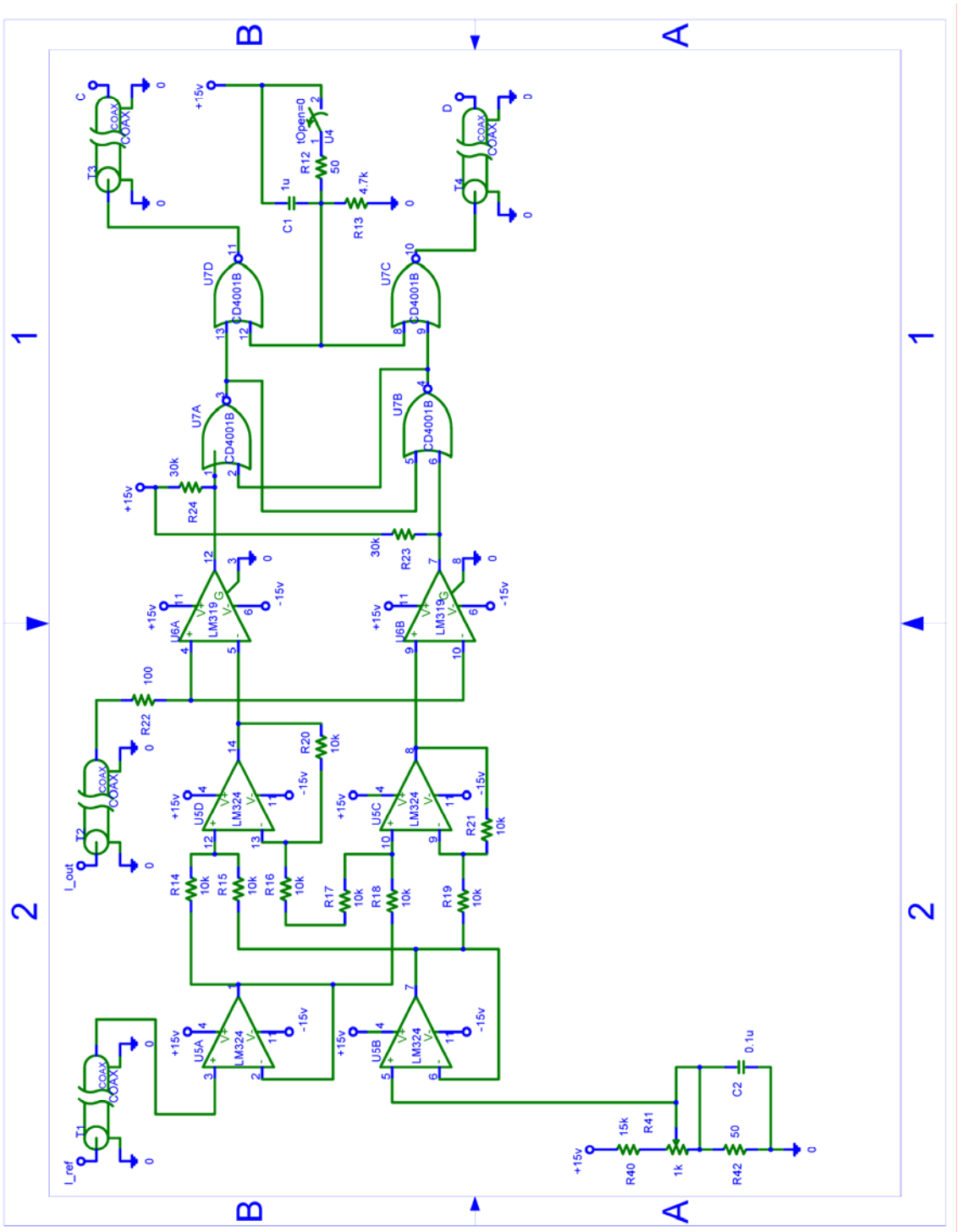


Figure 109. Hysteresis Circuit Schematic (One Phase Only)

Notes: 1) 100μF capacitor used in reset circuit to delay filter until bulk inverter is in steady state and 2) Reset switch feature not used on breadboard circuit

E. PARALLEL CONNECTED HYBRID INVERTERS (PCHI)

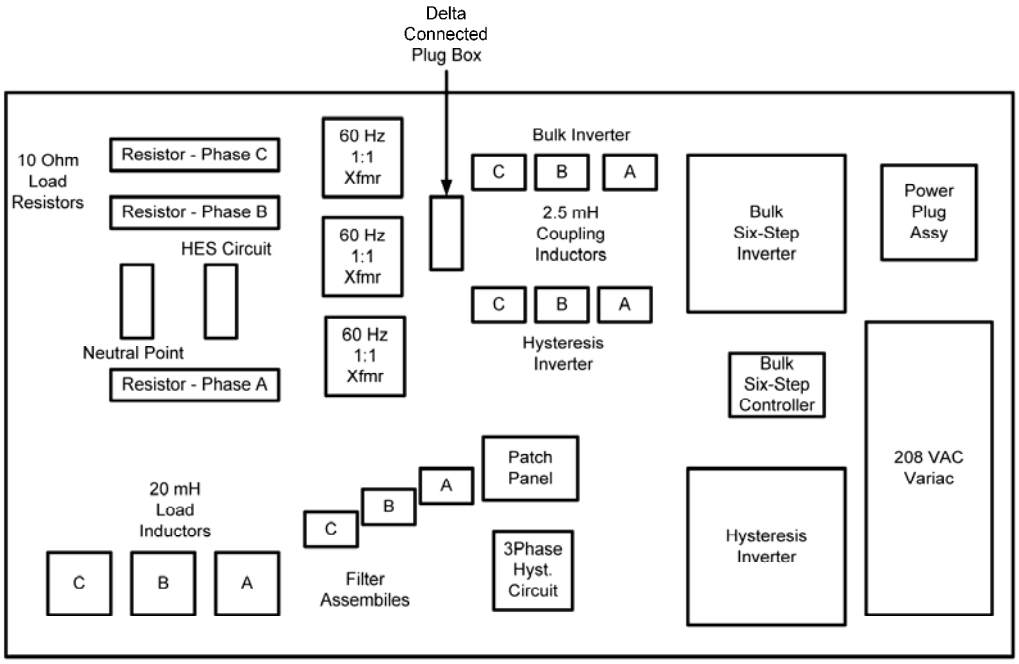


Figure 110. Lab Bench Setup Map

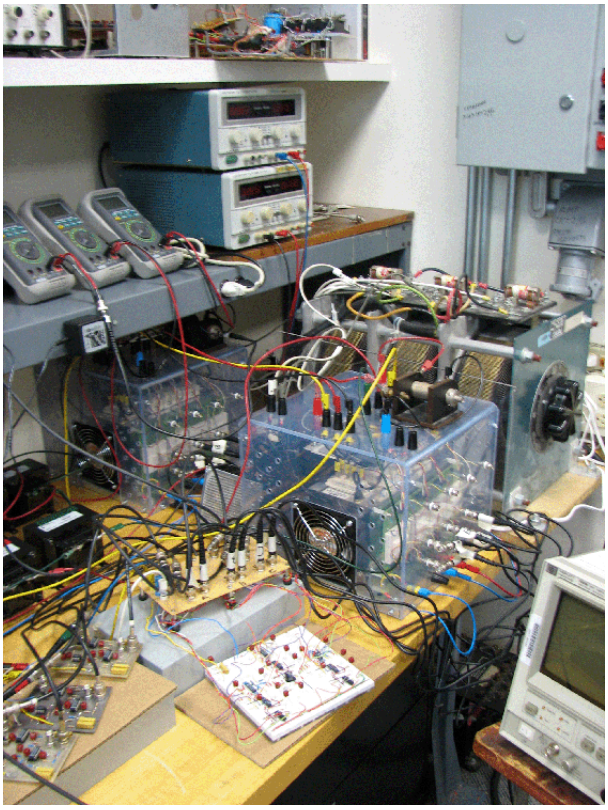


Figure 111. Power Supply Variac and both PEBBS

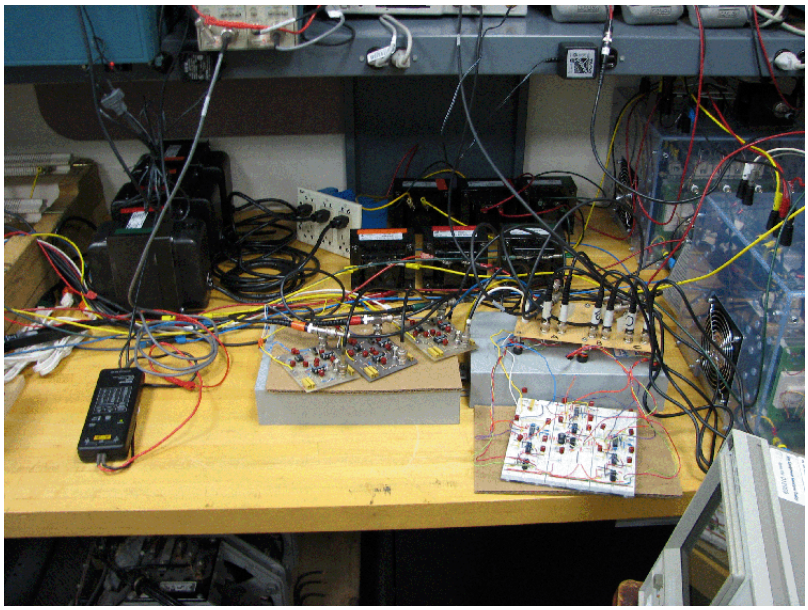


Figure 112. Hysteresis Controller and Inverter Coupling to Load

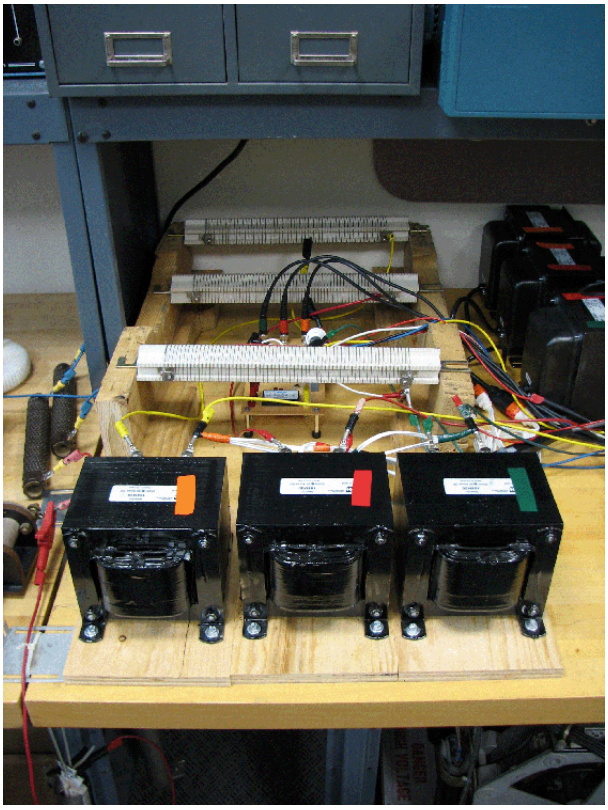


Figure 113. Three-phase Load and Hall Effect Sensors

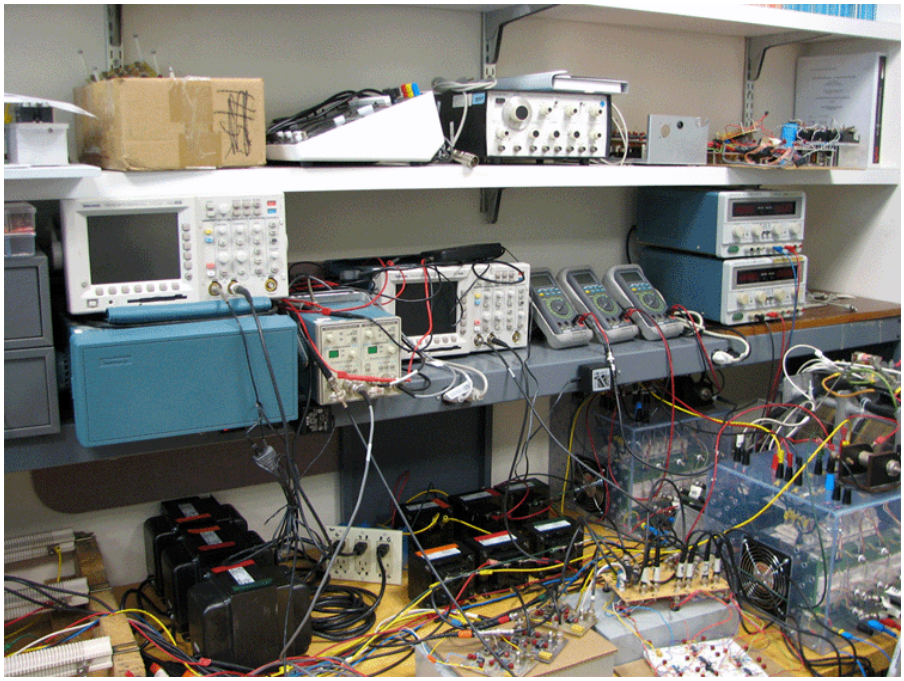


Figure 114. Test Equipment Used for Data Collection

F. PARTS LIST

Part	Qty	Value	Manufacturer	Description
Bulk Controller:				
74194	1	n/a	TI	Dip 16
7402	2	n/a	TI	Dip 14
7404	2	n/a	TI	Dip 14
7405	1	n/a	TI	Dip 14
LM555	1	n/a	National Semi	Dip 8
LM7805	1	n/a	National Semi	TO-92
LM7815	1	n/a	National Semi	TO-92
BNC Jacks	6	n/a	Amphenol	31-10
Banana Plugs	2	n/a	HH Smith	#205-103
C	5	0.01u	Digikey	
C	2	0.33u	Digikey	
R	6	620	Digikey	
R	4	1k	Digikey	
R	1	200k	Digikey	
Switch	1		Alco	MTA106F
Hall Effect Circuit:				
CLN-50	3	n/a	FW Bell	Hall-effect Sensors
DFC-10U24D15	1	n/a	Power One	+/- 15V Power Supply
C	2	1u	Digikey	Bypass Capacitors
R	3	100	Digikey	
Banana Plugs	5	n/a	HH Smith	#205-103
BNC Jacks	3	n/a	Amphenol	31-10
Hysteresis Filter:				
LM324	6	n/a	National Semi	Dip 14
LM1458	3	n/a	National Semi	Dip 8
C	27	1u	Digikey	
R	3	27	Digikey	
R	3	150	Digikey	
R	9	510	Digikey	
R	3	680	Digikey	
R	36	1k	Digikey	
R	3	2.4k	Digikey	
R	3	3.3k	Digikey	
R	3	8.2k	Digikey	
R	3	10k	Digikey	
Potentiometer	6	2k	Spectrol	43P202
Potentiometer	3	5k	Spectrol	43P202
BNC Jacks	9	n/a	AMP	part #: 414305-1
Banana Plugs	3	n/a	Pomona	part #: 1825-2
Hysteresis Circuit:			(Breadboard)	
LM324	3	n/a	National Semi	Dip 14
LM319	3	n/a	National Semi	Dip 14
CD4001	3	n/a	Fairchild	Dip 14
C	1	0.1u	Digikey	
C	16	1u	Digikey	
R	2	51	Digikey	
R	3	100	Digikey	
R	1	4.7k	Digikey	
R	24	10k	Digikey	
R	1	15k	Digikey	
R	6	30k	Digikey	
Potentiometer	1	2k	Spectrol	43P202
Switch	1	n/a	Alco	MTA106F
Load Elements:				
Coupling Inductors	6	2.5 mH	Hammond	195E30
Load Inductors	3	20 mH	Hammond	195M30
Isolation Transformers	3	60Hz	Hammond	171G

Table 17. Circuit Parts List

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